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13. ABSTRACT

To provide precise control of the fully steerable, 60-ft X-band antenna at the Naval Research Laboratory (NRL) Waldorf Microwave Space Research Facility (MSRF), a computer-oriented control system has been developed to control pointing of the antenna. The system has provisions for real-time data acquisition and processing for the control of experiments as well as for the display of antenna-related information such as antenna position, tracking object range, object look angles, and doppler frequency shift. Control equipment has been developed by NRL to provide the interface between the antenna system and the associated Control Data Corporation 924A general-purpose digital computer system. All control actions of the real-time system interface with the computer are transmitted to the desired equipment through logic circuits in the interface system. The computer system has been provided with a unique logic system for data acquisition and display. This capability allows the computer to acquire and convert analog data to digital form in real time via the interface system so that real-time processing may be used to modify experimental parameters. Alternatively, the acquired digital data may be stored for later processing in other computer systems.

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Computer control of microwave antenna Digital logic for radar antenna control						

CONTENTS

ABSTRACT

To provide precise control of the fully steerable, 60-ft X-band antenna at the Naval Research Laboratory (NRL) Waldorf Microwave Space Research Facility (MSRF), a computer-oriented control system has been developed to control pointing of the antenna. The system has provisions for real-time data acquisition and processing for the control of experiments as well as for the display of antenna-related information such as antenna position, tracking object range, object look angles, and doppler frequency shift. Control equipment has been developed by NRL to provide the interface between the antenna system and the associated Control Data Corporation 924A general-purpose digital computer system. All control actions of the real-time system interface with the computer are transmitted to the desired equipment through logic circuits in the interface system. The computer system has been provided with a unique logic system for data acquisition and display. This capability allows the computer to acquire and convert analog data to digital form in real time via the interface system so that real-time processing may be used to modify experimental parameters. Alternatively, the acquired digital data may be stored for later processing in other computer systems.

PROBLEM STATUS

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AUTHORIZATION

NRL Problem R01-36
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THE NRL MICROWAVE SPACE RESEARCH FACILITY

COMPUTER SYSTEM HARDWARE FOR DATA ACQUISITION AND CONTROL OF THE 60-FT X-BAND ANTENNA

INTRODUCTION

With the increased emphasis on satellite communications for use by the Navy within the Fleet, a facility has been developed to perform research in this area of communications. The facility includes a 60-ft X-band antenna system* (see Figs. 1 and 2) with associated receiving and transmitting systems and the Navy Antenna Computer Tracking and Command (NACTAC) system consisting of a general-purpose digital computer, Control Data Corporation (CDC) 924A, and the NRL-designed interface to the antenna system.

Precise program tracking of both active and passive satellites, as well as celestial objects, was assigned to the computer and was accomplished through special hardware and computer software developed by NRL.

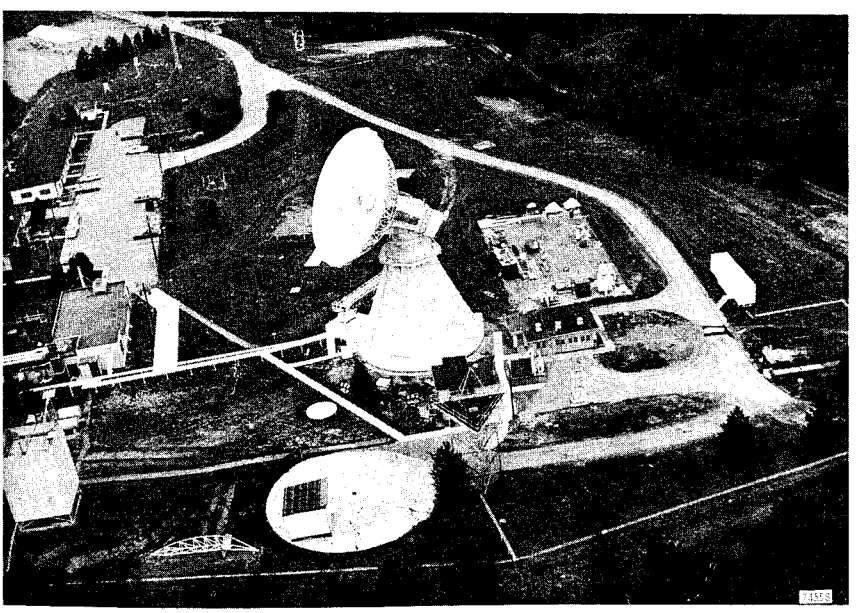

Fig. 1 - NRL Waldorf Microwave Space Research Facility

*Bass, C.A., and Townsend, D.H., "The NRL Microwave Space Research Facility: Design and Development of the 60-ft X-Band Antenna," NRL Report 6921, Aug. 11, 1969

Fig. 2 - Sixty-foot X-band antenna

Through use of this computer system and its associated software and interface, it is possible to control the pointing of the antenna to a resolution of 0.001 degree and to accurately track objects at velocities from 1/10 sidereal rate to 6 deg/sec, as well as provide displays of all pertinent antenna and experiment related information. The computer system also controls all antenna scanning functions and the acquisition of the object being tracked.

While control of the antenna is the primary function of the computer system, it is also used for such secondary purposes as real-time acquisition and processing of experimental data. A further capability is control of synthesizers which establish the receiving and transmitting frequencies of the station.

Both hardware and software functions of the NACTAC system are shown in Fig. 3. This report deals for the most part with hardware aspects of the real-time digital system. The software portions and operating procedures are to be described in detail in subsequent reports in preparation.

COMPUTER HARDWARE

The CDC 924A computer associated with the NACTAC system is a stored-program, general-purpose digital computer, incorporating second-generation hardware of the type used in the CDC 1604-160 series computers.

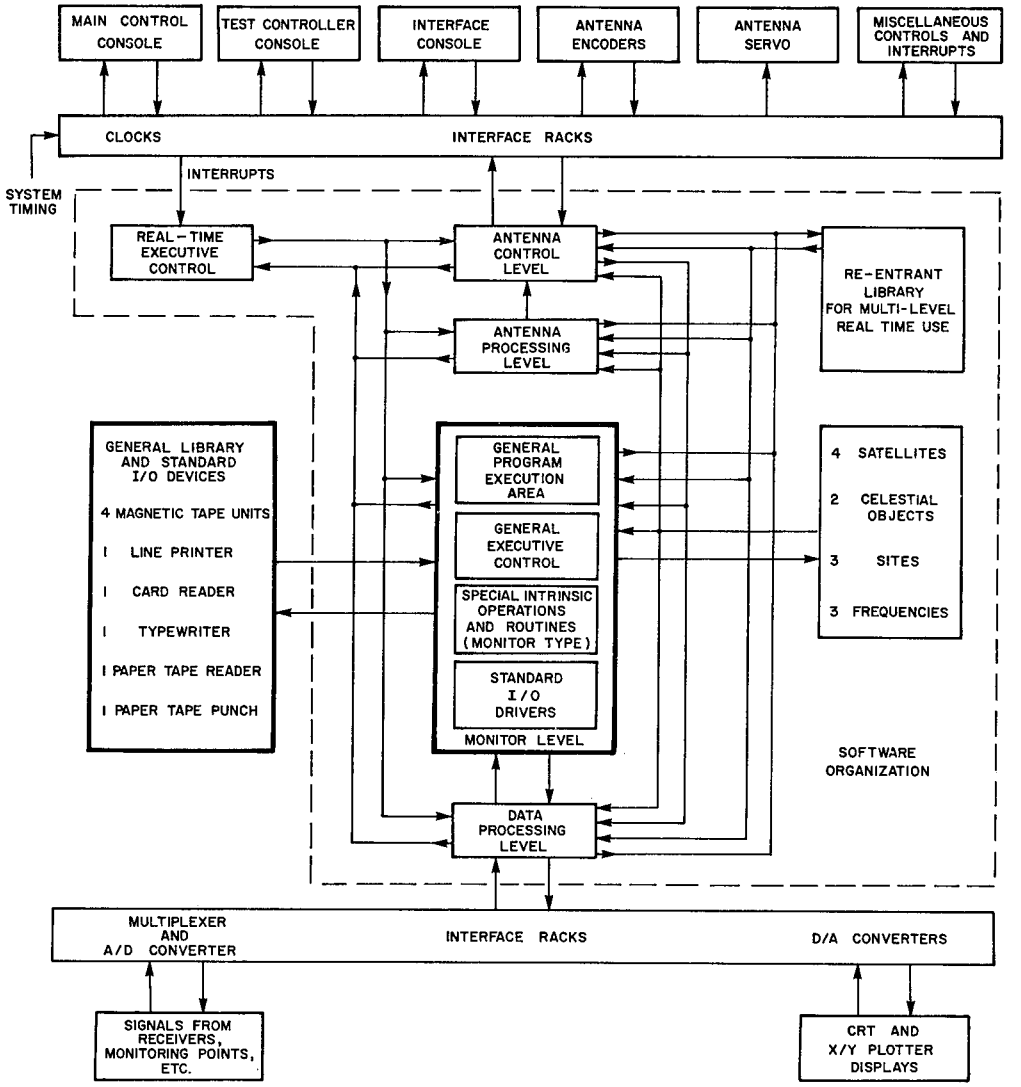

Fig. 3 - NACTAC System

The following is a sample of the computer's characteristics:

Mode	Parallel
Word length	24 bits
Storage	Core, 16,384 words
Total cycle Time	4.8 μsec
I/O Channels	Six—3 input, 3 output
I/O Modes	Three—160 (12 bit), 924 (24 bit), 1604 (48 bit)
Arithmetic	Binary modulus 2^{24}-1 (one's complement)
Instructions	See Appendix A
Index registers	Six

The total cycle time quoted, which was previously 6.4 μsec for the CDC-924A computer, is the result of the addition of a speed-up modification which, because of the improved cycle time, has also increased the input-output (I/O) data transfer rate. While at present only 16,384 words of storage are provided, the computer's storage capability may be expanded to 32,768 words.

Tables 1 and 2 list the operational registers in the computer and their arithmetic properties.

Table 1
Operational Registers Associated With
the CDC-924A Computer

Register	Function
A	Arithmetic
Q	Auxiliary arithmetic
B^1 through B^6	Index registers (six)
P	Program address
U	Program control

Table 2
Arithmetic Properties of Operational Registers

Register	Number of Stages	Modulus	Complement Notation	Arithmetic	Result
A	24	$2^{24}-1$	one's	subtractive	signed
Q	24	$2^{24}-1$	one's	subtractive	signed
P	15	2^{15}	two's	additive	unsigned
U	15	2^{15}	two's	subtractive	unsigned

The 24 bit computer instruction word is of the single-address type and is logically broken into three segments as shown in Fig. 4.

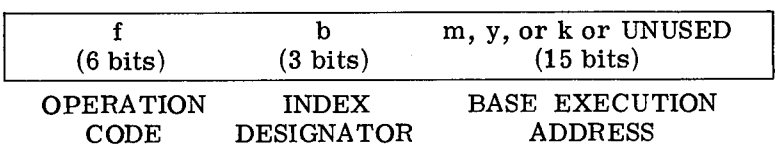

Fig. 4 - Instruction word division

The first six bits of the instruction word (highest order) contain the operation code which specifies the function to be performed by the computer. The next lower three bits contain the index designator which is used in relative address modification, in specifying the index whose contents are to be added to the execution address, and for indirect addressing. The lower 15 bits contain the execution address which is used as an operand address, an operand, or as a shift count. The CDC 924A instruction repertoire, a list of which is given in Appendix A, includes such functions as fixed-point arithmetic, logical and masking operations, indexing, I/O operations, jumps and stops, and storage searching.

The binary arithmetic performed by the 924A is accomplished in ones' complement form modulus $2^{24}-1$. Full word arithmetic operations include addition, subtraction, integer multiplication and division, and such address arithmetic operations as increasing or decreasing registers. Also incorporated is a modification to perform fractional multiplication.

The computer system, as associated with NACTAC, consists of main frame, operating console, Model 161 typewriter, Model 167-2 card reader, Model 166-2 line printer, Model 925 tape synchronizer, and four Model 603 tape handlers.

Main Frame

All control logic and the magnetic core memory are located within the main frame, which is plenum cooled with an internal fan for circulating cool air from the plenum. This unit contains approximately 1200 printed circuit cards as well as the two magnetic core storage units, each of which have a capacity of 8,192 words. All control and information cables are passed through the plenum for connection to the console and to peripheral equipment.

Operating Console

The contents of all previously described registers are displayed on the operating console (Fig. 5a) in octal form using in-line, projection-type displays. The memory may be modified or monitored through use of the program address register (P register) and program control register (U register). Manual input to the registers may be accomplished by use of momentary-action pushbutton switches associated with each bit in a register. In addition, provisions have been included for manual stepping of programs, manual input of instructions, and control of all programmable jump and stop instructions.

Located on the operator's console is the CDC Model 350 photoelectric paper tape reader, which will read 5-, 7-, or 8-level paper tapes of standard widths at a rate of 350 characters per second. Direct access from the tape reader to memory may be accomplished in a reader load mode.

Located in the lower left side of the console is a high-speed paper tape punch which will operate at a nominal rate of 110 characters per second. The tape punch must also be selected manually and buffered via software, there being no automatic output mode for this device. Both the paper tape reader and the paper tape punch must be operated on computer I/O Channels 1 and 2.

Also located on the operator's console is a set of five 8-position thumbwheel switches which provide the operator with a means of stopping the computer prior to the execution of an instruction located in any desired memory location.

Typewriter Model 161

The CDC Model 161 typewriter (Fig. 5b) consists of an electric typewriter and a control chassis which includes a coder/decoder, and operates only in 160 mode (12 bits). Both the typewriter and control chassis are located in a separate stand and are connected to computer I/O Channels 1 and 2, 160 mode, via plenum cabling. All typewriter characters and functions are represented by unique combinations of 6 bits, which are buffered from the typewriter one 6-bit character per 12-bit word at a maximum rate of 12 characters/second.

Card Reader Model 167-2

The CDC 167-2 card reader (Fig. 5c) reads data from standard punched cards and transfers it to the computer in the on-line mode, or to either the 166-2 line printer or

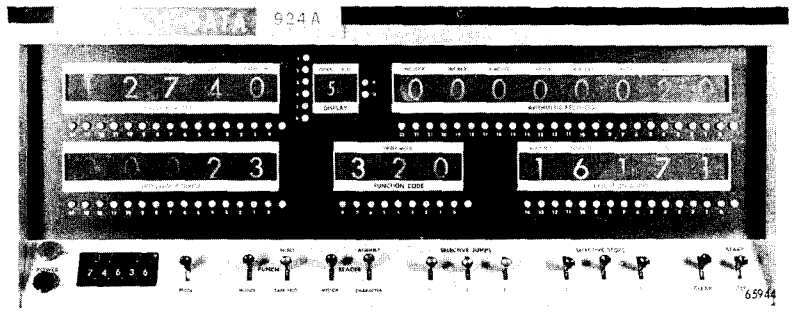

Fig. 5a - Computer operating console

Fig. 5b - Model 161 typewriter

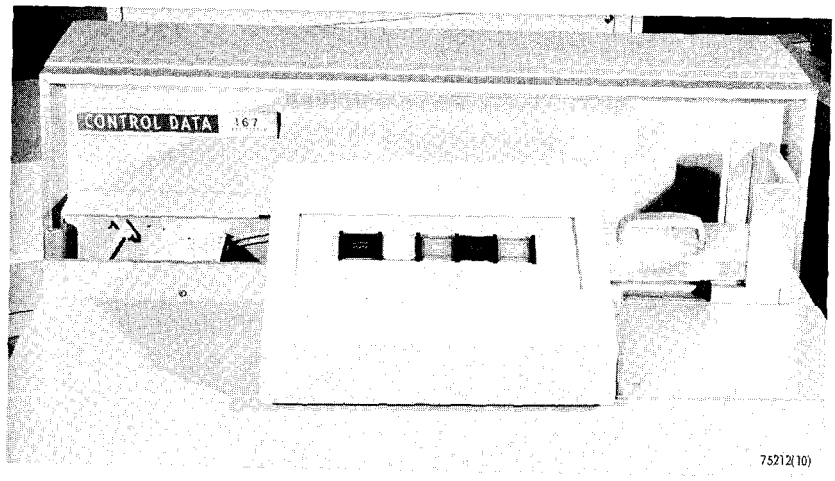

Fig. 5c - Model 167 card reader

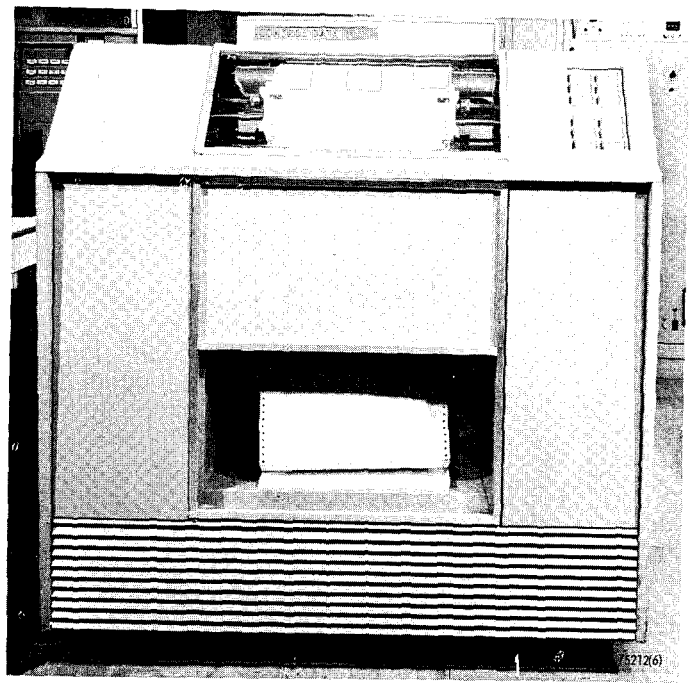

Fig. 5d - Model 166-2 line printer

the 925 magnetic tape synchronizer in an off-line mode. Data is read column by column and sent to the selected equipment as a 12-bit word in either Hollerith or BCD formats, the latter being the result of an internal translator which may be selected under program control. For the BCD mode, two Hollerith columns are translated to two 6-bit BCD characters and are then packed into one 12-bit word. While the card reader is capable of operating through any of the computer input channels in 160 mode, in the NACTAC system it is operated only through Channel 1. A modification made to the 167-2 card reader by NRL consists of a switch and a 51-pole, form C relay for disconnecting the card reader from the on-line equipment when the card reader is being operated as an off-line device. Activating the switch causes the relay to disconnect all the control and data lines of the card reader from computer I/O Channels 1 and 2 and connects them directly to off-line circuitry in the line printer.

Line Printer Model 166-2

The 166-2 line printer (Fig. 5d) which includes provisions for off-line as well as on-line operation, has a maximum line width of 120 characters and a maximum printing speed of 150 lines per minute using a 64-character drum. The fully buffered printer contains a magnetic core storage with a capacity of eighty 12-bit words.

Operating modes for the 166-2 line printer include two on-line modes, synchronous and asynchronous, and three off-line modes which provide information transfer for magnetic tape to printer (asynchronous), card reader to printer (asynchronous), and card reader to magnetic tape.

Magnetic Tape Synchronizer Model 925

The Control Data 925 tape synchronizer (Fig. 6a) is the controlling device for the four CDC 603 magnetic tape handlers, and will operate both on-line and off-line. Separate read-write circuitry in the 925 allow simultaneous read and write operation with two tape handlers while operating on-line. During off-line operation the 166-2 line printer controls information transfer and tape motion.

Tape Handler Model 603

Four magnetic tape handlers (Fig. 6b) are connected to on-line or off-line equipment through the tape synchronizer; each of them may be set to any of five logical unit numbers from 0 through 4. Logical units 1 through 4 are used as on-line devices, whereas logical unit 0 is used only while operating off-line. Data may be written in binary format as it is represented in core storage or in BCD format as represented in core by a 6-bit binary number in either of two densities, 556 frames/inch or 200 frames/inch. The maximum handler read/write speed is 75 ips, and each handler is equipped with manual controls for loading, rewinding, advancing tape, reversing, and unloading.

COMPUTER-ANTENNA INTERFACE

General Description

The computer interface, which serves as a central input and output control between the antenna and the computer, was designed and developed by NRL using component assemblies built by several manufacturers. All digital information to and from the antenna terminates in the interface system. In addition, the equipment is also the point

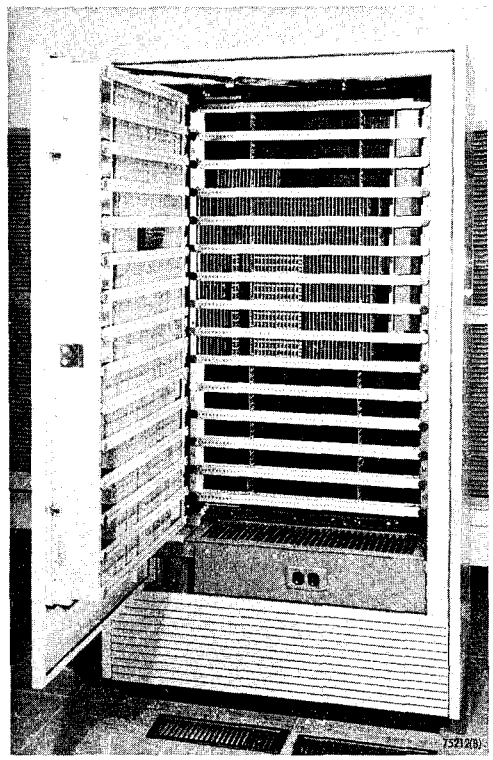

Fig. 6a - Model 925 tape synchronizer

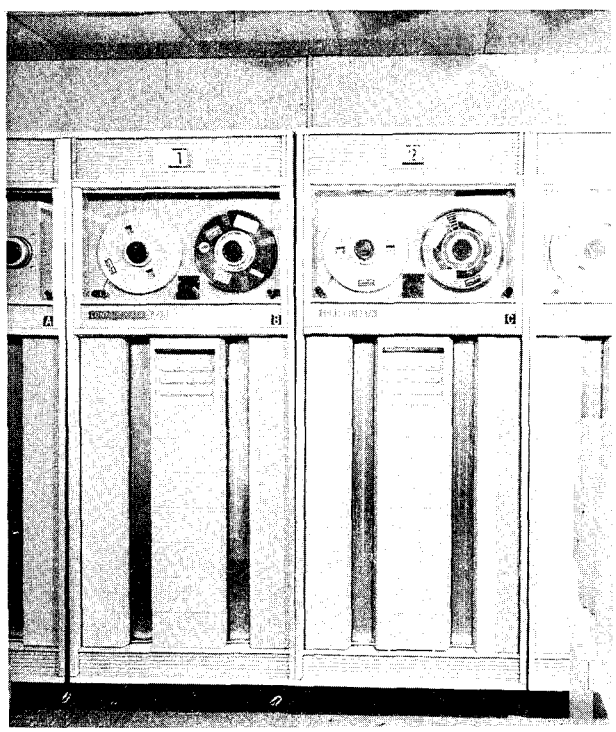

Fig. 6b - Model 603 tape handlers

of conversion for analog inputs to the computer which must be converted to digital form. The equipment, including the analog conversion devices, is located in a four-cabinet bay in the computer and antenna control room of the Waldorf Microwave Space Research Facility (WMSRF).

Figure 7a is a view of the computer interface equipment bay and gives a general view of the layout of this equipment. Figure 7b shows the layout of the computer center in the control room.

The interface equipment incorporates S-pac, NAND-type negative logic, manufactured by the Computer Control Company (3C) Division of Honeywell and, except for one card type, all logic is made up of off-the-shelf circuit cards.

Three basic sections of the interface equipment consist of: (a) antenna-computer communication and control operating through computer I/O Channels 3 and 4; (b) data acquisition and display operating through computer I/O Channels 5 and 6; and (c) miscellaneous components such as clocks, control panels, and power distribution.

Channels 3 and 4 are used almost exclusively for control of the antenna and the sampling and display of such parameters as range, range rate, position, scan conditions, and angle offsets. All commands to the antenna from the operator in digital mode are inputed to the computer through Channel 3 and are outputed either to the antenna servo or antenna control panel by the computer through Channel 4. Channel 3 is used by the computer to interrogate the antenna system's digital angle encoder and to transfer the information at the output of the encoder to the computer after it is interrogated.

All switches located on the various control panels associated with the Channel 3 and 4 interface equipment are sensed by the computer through the interface, and all action is taken by software, with the exception of the real-time and data-acquisition sampling clock controls, which are hardware connected.

To allow for analog as well as digital input to the computer, the interface system has been provided with separate circuitry on Channels 5 and 6 for the acquisition of analog data and the subsequent conversion to digital form. Equipment associated with this section of the interface includes a 160-channel, randomly addressable multiplexer and a 12-bit analog-to-digital (A/D) converter connected through logic to equipment in Channel 5. Also included for the purpose of calibration is a precision dc voltage source with seven selectable voltages, the output of which may be connected to all channels of the multiplexer simultaneously to calibrate the A/D converter. The D/A converter may then be calibrated through use of a special loop test which outputs a digital word from the computer corresponding to a fixed voltage to the D/A converter. The output of the D/A converter is then sampled by the calibrated A/D converter and the resulting digital word is compared by software for calibration purposes.

System Clocks

The main system clock is a real-time clock which is used to display GMT on all three control panels (see Fig. 8) in addition to the antenna control console (see Fig. 9). Included as an integral part of the station is a master station clock which is synchronized to WWV and used to synchronize the main system clock. The input signal to both clocks is derived from precision frequency standards which are controlled by a cesium-beam standard. In addition to driving the clock displays, the main system clock supplies output pulses at rates of 2^1 pps to 2^9 pps in increasing powers of 2 for use as strobe, sample, and interrupt functions. Since there is no software control provided, the clock is preset, started, and stopped by switches connected directly to control logic.

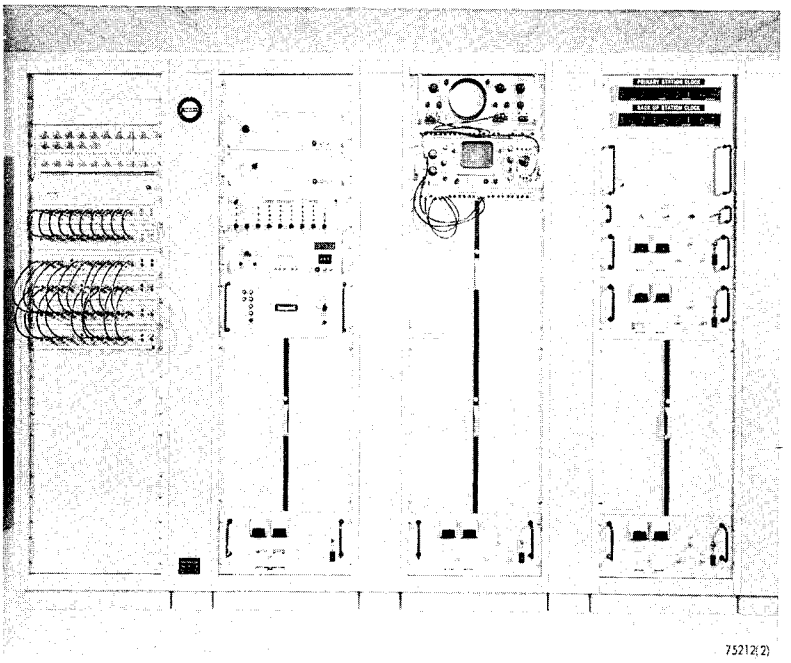

Fig. 7a - Computer interface bay

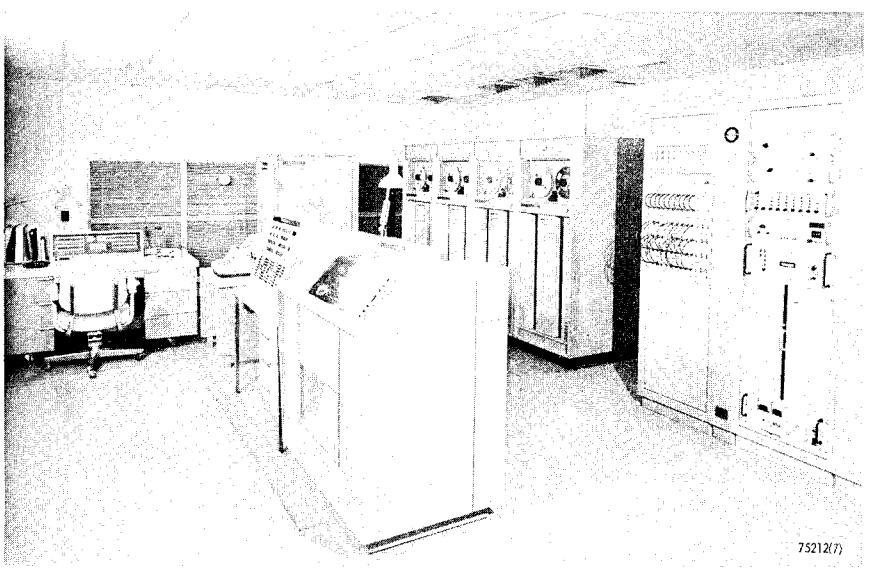

Fig. 7b - Waldorf MSRF computer center layout

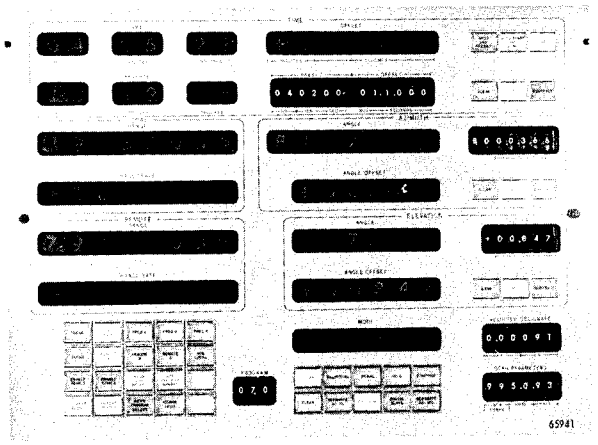

Fig. 8a - Main control panel

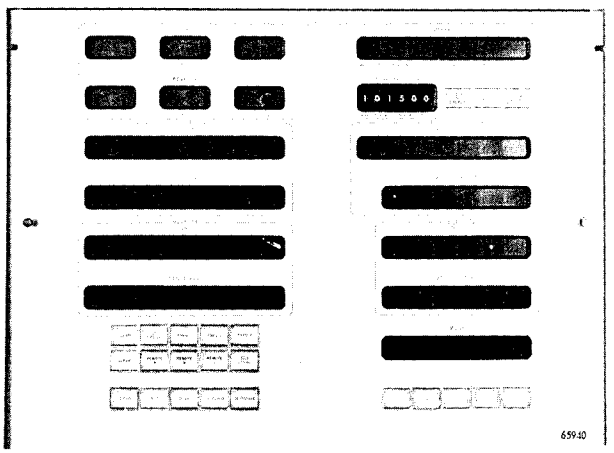

Fig. 8b - Test controller's panel

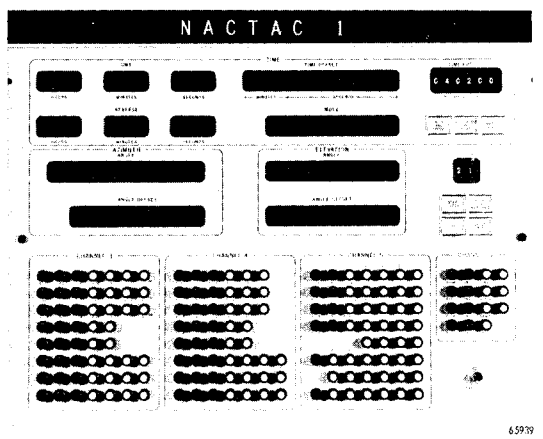

Fig. 8c - Computer console panel

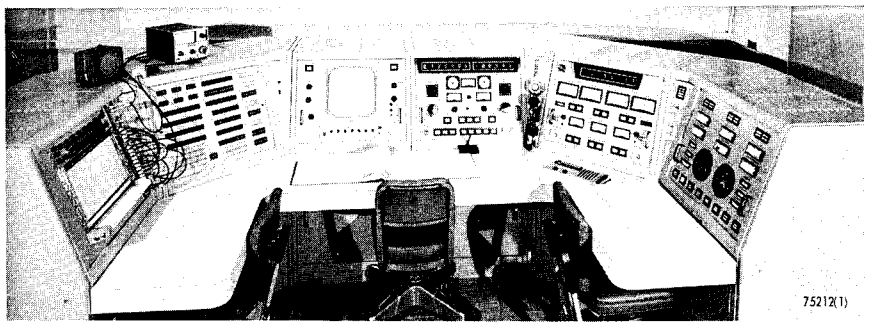

Fig. 9 - Antenna control console

In addition to the real-time clock there is a reverse or countdown clock associated with the system which, unlike the GMT clock, must be controlled completely by software. The preset information is entered through thumbwheel switches located on the test controller's console (Fig. 8b) and, upon selection of the proper function code, the reverse clock is preset to the setting of the thumbwheel switch. No action occurs until the computer, after having sensed through software that the start switch has been depressed, sends a function code to the interface to start the clock. In addition, the clock may also be preset and started at the discretion of software. The input to the reverse clock is a 1-pps square wave supplied by the system real-time clock, which causes the reverse clock to count down to zero. In addition to visual indication, an interrupt is available to alert the computer when the reverse clock has completed its countdown. Like the real-time clock, the reverse clock is displayed on all three control consoles (see Fig. 8).

For purposes of digital data acquisition and display, a variable data-conversion clock has been provided which, when activated, controls the data sampling conversion rates. The variable clock is used exclusively with Channels 5 and 6 and will be described in more detail in the discussion of Channels 5 and 6 equipment.

Control Panels

Three control panels are associated with the NACTAC interface system, each having its own unique function. The main control console (Fig. 8a), located in one bay of the antenna control console (Fig. 9), is used to input antenna commands to the computer in the digital mode. The displays available on this panel are

Antenna azimuth
Antenna elevation
GMT clock
Reverse clock
Time offset
Azimuth offset
Elevation offset
Local site range
Local site range rate
Remote site range
Remote site range rate
Mode display.

Also provided on the main control panel are groups of switches for data and command inputs associated with the control of the antenna in the digital mode. These switch groups are

Mode switches (designate az-el, program track, etc.)
Scan selection and initiation (spiral, elliptical, etc.)
Scan parameters (increment, amplitude, and rate)
Antenna angle designation and offsets
Display, cam, and acquisition control program selection
Local range and range-rate display
Remote range and range-rate display
Receiver selection.

None of the switches associated with this panel are hardware connected with the exception of the controls for the real-time clock. All commands for action are inputed to the computer by sensing switch conditions. After software interpretation, the computer then responds by performing the requested function, if valid, and setting the switch light.

The range and range-rate control switches are used to signal the computer to apply lamp power to the selected display and to select the proper quantity for display. The range and range-rate displays serve a dual purpose, to provide range information in Earth radii and range rate as monostatic doppler shift in Hz/GHz, or to display both the path loss as free space attenuation in dB between isotropic antennas and range rate in hertzes for a selected frequency.

The test controller's panel (Fig. 8b) is located in one bay of the test controller's console and is used to monitor the action of the antenna during an experiment. It is from this panel that the reverse clock and any desired computer control of the experiment being performed is activated. Displays available on this panel are identical to those on the main control panels described previously.

Control switches located on this panel are

Reverse clock preset, stop, and start
Local range and range-rate display
Remote range and range-rate display
Quick look initiation
Computer experiment control switches.

The range and range-rate switches on this panel perform functions identical to those on the main control panel.

The quick-look initiation switches allow the operator to obtain look angles for the object to be tracked without outputing to the line printer. This feature allows the operator to advance or decrease the selected time in operator-selected increments to determine present and future pointing angles, range, and range-rate corresponding to the orbital path of a desired object, the parameters of which have been entered into memory. All actions of these switches are subject to the antenna operation not being in digital mode.

The computer experiment control switches allow the operator to control the experiment via the computer once the appropriate software defining the action desired for each switch has been provided. This feature permits flexible use of the computer to perform or assist in experiments.

The computer control panel (Fig. 8c) is located in a desk console in close proximity to the computer's operating console (see Fig. 7b), and is used to monitor the operations taking place in the interface. Most function codes have an associated lamp located on this panel which provides the operator with a cursory view of internal operations. This panel is used mainly for trouble shooting, debugging, and monitoring general operations. Displays available on this panel are

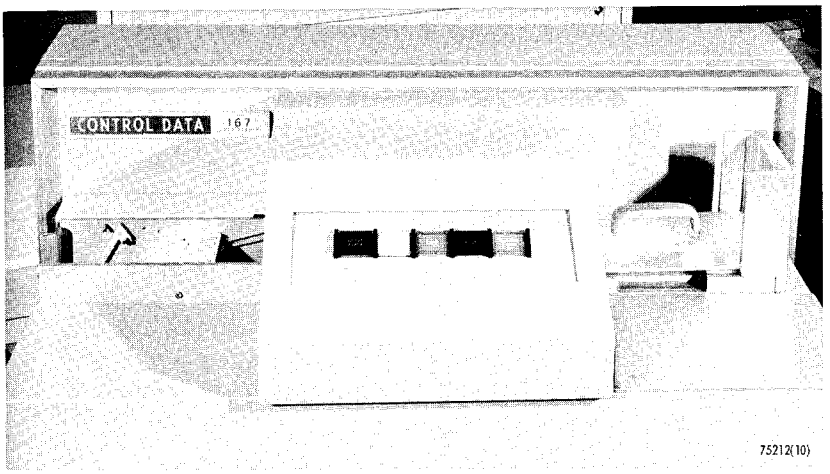

Fig. 5c - Model 167 card reader

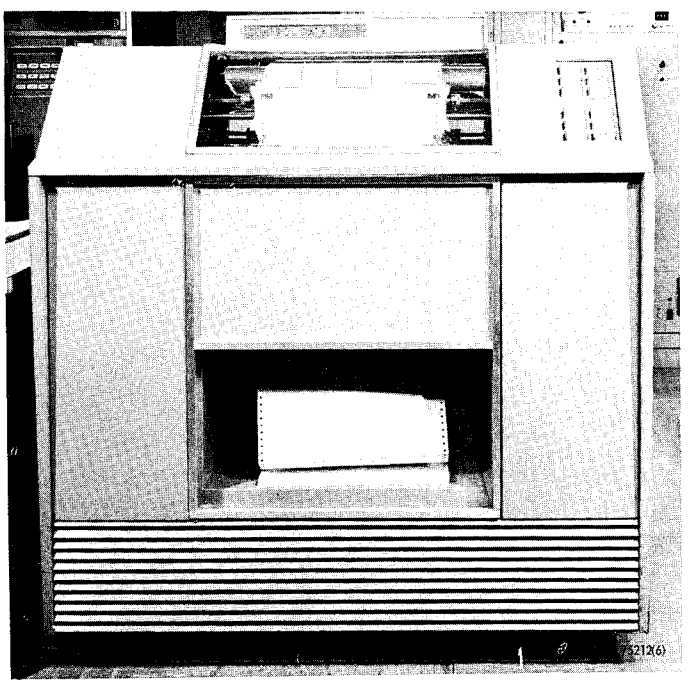

Fig. 5d - Model 166-2 line printer

the 925 magnetic tape synchronizer in an off-line mode. Data is read column by column and sent to the selected equipment as a 12-bit word in either Hollerith or BCD formats, the latter being the result of an internal translator which may be selected under program control. For the BCD mode, two Hollerith columns are translated to two 6-bit BCD characters and are then packed into one 12-bit word. While the card reader is capable of operating through any of the computer input channels in 160 mode, in the NACTAC system it is operated only through Channel 1. A modification made to the 167-2 card reader by NRL consists of a switch and a 51-pole, form C relay for disconnecting the card reader from the on-line equipment when the card reader is being operated as an off-line device. Activating the switch causes the relay to disconnect all the control and data lines of the card reader from computer I/O Channels 1 and 2 and connects them directly to off-line circuitry in the line printer.

Line Printer Model 166-2

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Operating modes for the 166-2 line printer include two on-line modes, synchronous and asynchronous, and three off-line modes which provide information transfer for magnetic tape to printer (asynchronous), card reader to printer (asynchronous), and card reader to magnetic tape.

Magnetic Tape Synchronizer Model 925

The Control Data 925 tape synchronizer (Fig. 6a) is the controlling device for the four CDC 603 magnetic tape handlers, and will operate both on-line and off-line. Separate read-write circuitry in the 925 allow simultaneous read and write operation with two tape handlers while operating on-line. During off-line operation the 166-2 line printer controls information transfer and tape motion.

Tape Handler Model 603

Four magnetic tape handlers (Fig. 6b) are connected to on-line or off-line equipment through the tape synchronizer; each of them may be set to any of five logical unit numbers from 0 through 4. Logical units 1 through 4 are used as on-line devices, whereas logical unit 0 is used only while operating off-line. Data may be written in binary format as it is represented in core storage or in BCD format as represented in core by a 6-bit binary number in either of two densities, 556 frames/inch or 200 frames/inch. The maximum handler read/write speed is 75 ips, and each handler is equipped with manual controls for loading, rewinding, advancing tape, reversing, and unloading.

COMPUTER-ANTENNA INTERFACE

General Description

The computer interface, which serves as a central input and output control between the antenna and the computer, was designed and developed by NRL using component assemblies built by several manufacturers. All digital information to and from the antenna terminates in the interface system. In addition, the equipment is also the point

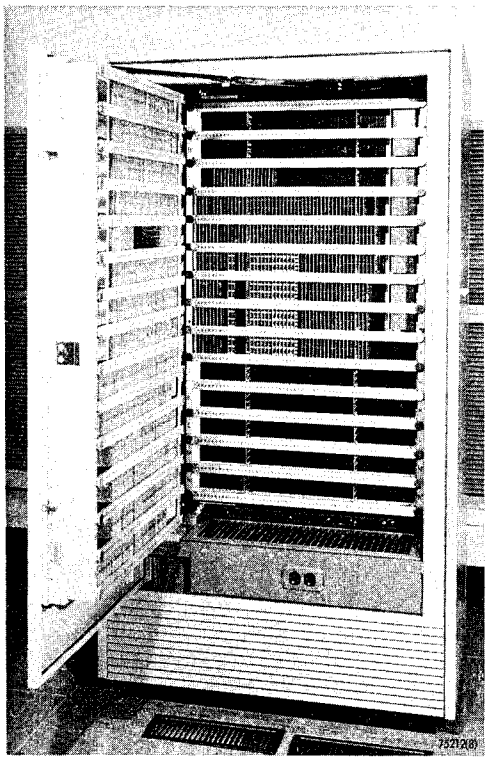

Fig. 6a - Model 925 tape synchronizer

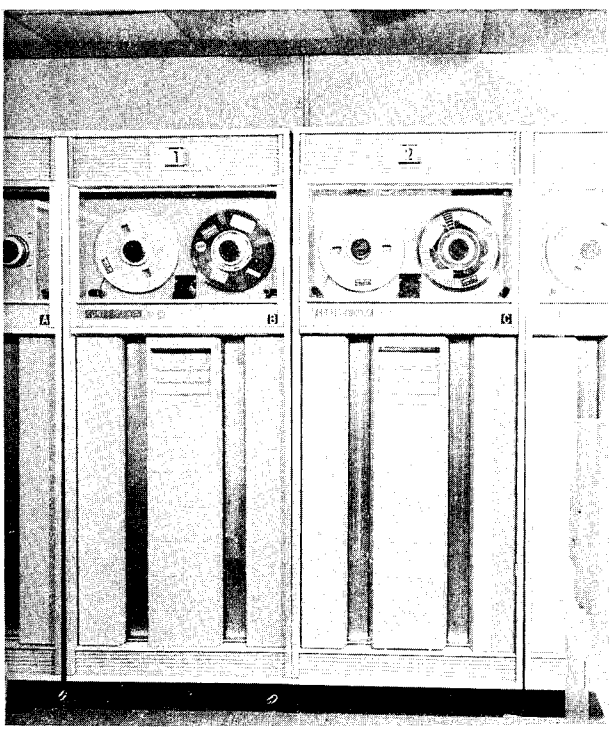

Fig. 6b - Model 603 tape handlers

of conversion for analog inputs to the computer which must be converted to digital form. The equipment, including the analog conversion devices, is located in a four-cabinet bay in the computer and antenna control room of the Waldorf Microwave Space Research Facility (WMSRF).

Figure 7a is a view of the computer interface equipment bay and gives a general view of the layout of this equipment. Figure 7b shows the layout of the computer center in the control room.

The interface equipment incorporates S-pac, NAND-type negative logic, manufactured by the Computer Control Company (3C) Division of Honeywell and, except for one card type, all logic is made up of off-the-shelf circuit cards.

Three basic sections of the interface equipment consist of: (a) antenna-computer communication and control operating through computer I/O Channels 3 and 4; (b) data acquisition and display operating through computer I/O Channels 5 and 6; and (c) miscellaneous components such as clocks, control panels, and power distribution.

Channels 3 and 4 are used almost exclusively for control of the antenna and the sampling and display of such parameters as range, range rate, position, scan conditions, and angle offsets. All commands to the antenna from the operator in digital mode are inputed to the computer through Channel 3 and are outputed either to the antenna servo or antenna control panel by the computer through Channel 4. Channel 3 is used by the computer to interrogate the antenna system's digital angle encoder and to transfer the information at the output of the encoder to the computer after it is interrogated.

All switches located on the various control panels associated with the Channel 3 and 4 interface equipment are sensed by the computer through the interface, and all action is taken by software, with the exception of the real-time and data-acquisition sampling clock controls, which are hardware connected.

To allow for analog as well as digital input to the computer, the interface system has been provided with separate circuitry on Channels 5 and 6 for the acquisition of analog data and the subsequent conversion to digital form. Equipment associated with this section of the interface includes a 160-channel, randomly addressable multiplexer and a 12-bit analog-to-digital (A/D) converter connected through logic to equipment in Channel 5. Also included for the purpose of calibration is a precision dc voltage source with seven selectable voltages, the output of which may be connected to all channels of the multiplexer simultaneously to calibrate the A/D converter. The D/A converter may then be calibrated through use of a special loop test which outputs a digital word from the computer corresponding to a fixed voltage to the D/A converter. The output of the D/A converter is then sampled by the calibrated A/D converter and the resulting digital word is compared by software for calibration purposes.

System Clocks

The main system clock is a real-time clock which is used to display GMT on all three control panels (see Fig. 8) in addition to the antenna control console (see Fig. 9). Included as an integral part of the station is a master station clock which is synchronized to WWV and used to synchronize the main system clock. The input signal to both clocks is derived from precision frequency standards which are controlled by a cesium-beam standard. In addition to driving the clock displays, the main system clock supplies output pulses at rates of 2^1 pps to 2^9 pps in increasing powers of 2 for use as strobe, sample, and interrupt functions. Since there is no software control provided, the clock is preset, started, and stopped by switches connected directly to control logic.

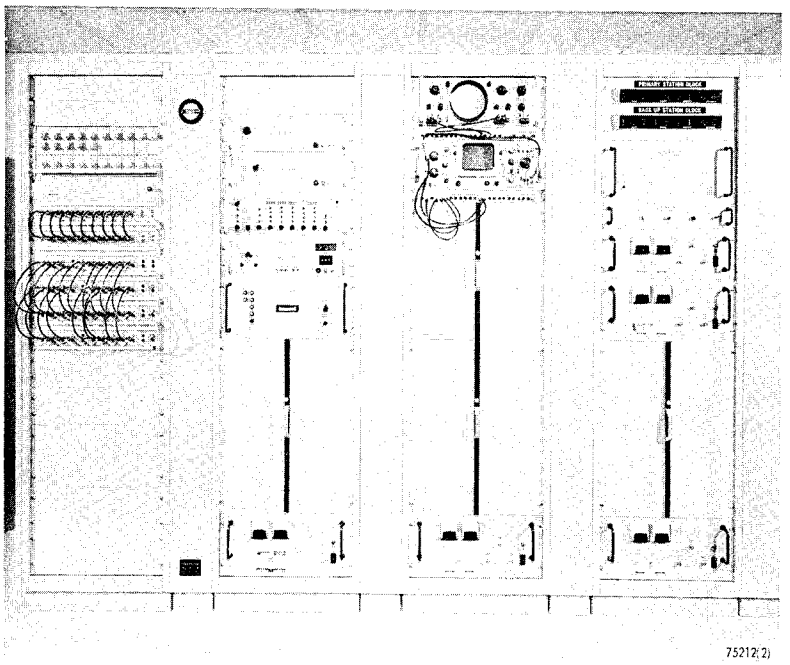

Fig. 7a - Computer interface bay

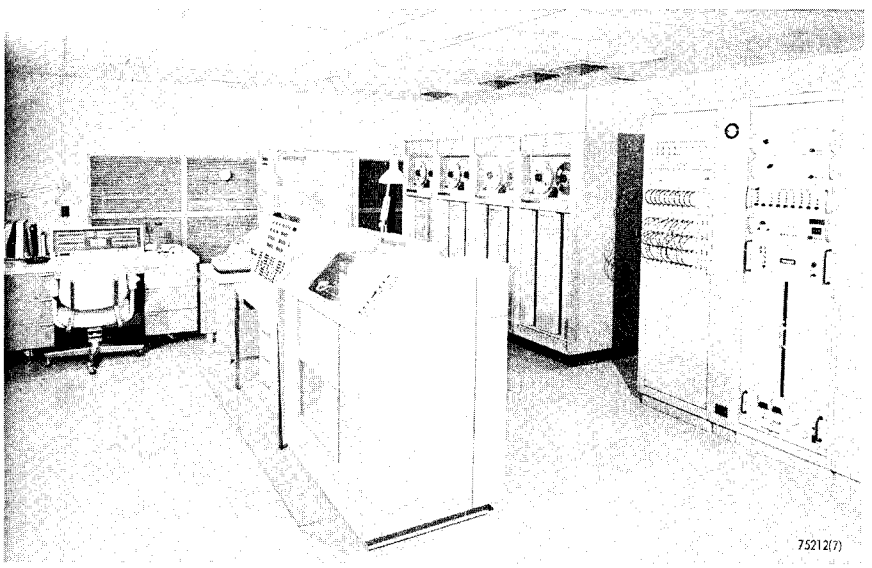

Fig. 7b - Waldorf MSRF computer center layout

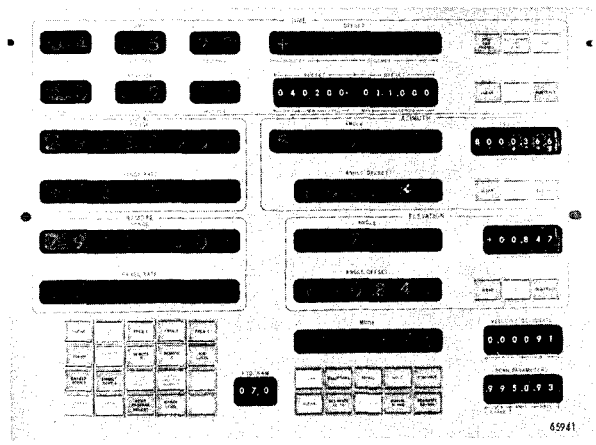

Fig. 8a - Main control panel

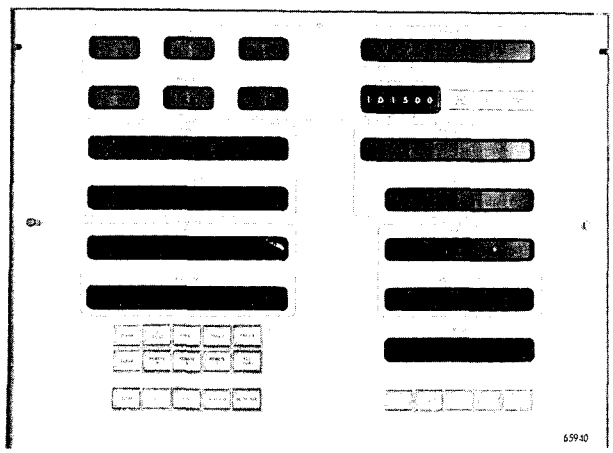

Fig. 8b - Test controller's panel

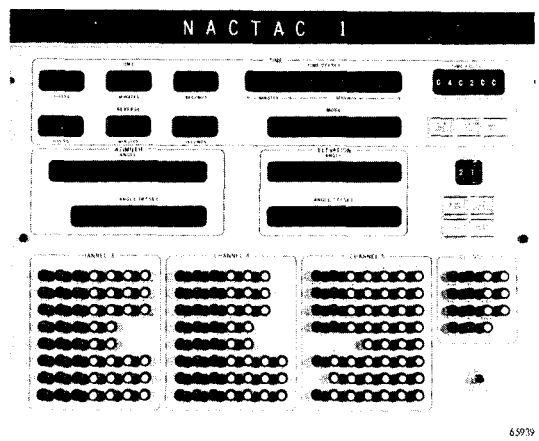

Fig. 8c - Computer console panel

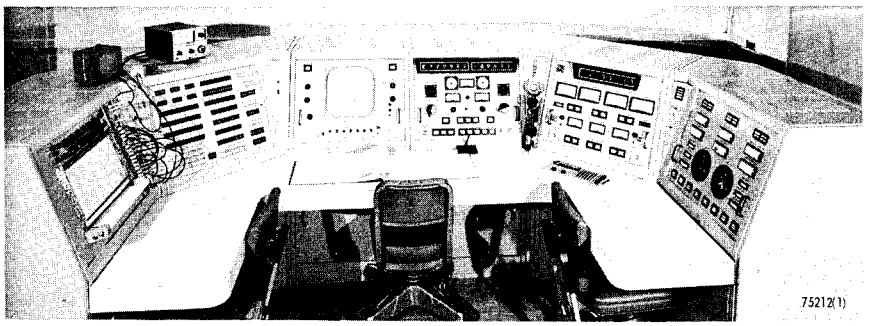

Fig. 9 - Antenna control console

In addition to the real-time clock there is a reverse or countdown clock associated with the system which, unlike the GMT clock, must be controlled completely by software. The preset information is entered through thumbwheel switches located on the test controller's console (Fig. 8b) and, upon selection of the proper function code, the reverse clock is preset to the setting of the thumbwheel switch. No action occurs until the computer, after having sensed through software that the start switch has been depressed, sends a function code to the interface to start the clock. In addition, the clock may also be preset and started at the discretion of software. The input to the reverse clock is a 1-pps square wave supplied by the system real-time clock, which causes the reverse clock to count down to zero. In addition to visual indication, an interrupt is available to alert the computer when the reverse clock has completed its countdown. Like the real-time clock, the reverse clock is displayed on all three control consoles (see Fig. 8).

For purposes of digital data acquisition and display, a variable data-conversion clock has been provided which, when activated, controls the data sampling conversion rates. The variable clock is used exclusively with Channels 5 and 6 and will be described in more detail in the discussion of Channels 5 and 6 equipment.

Control Panels

Three control panels are associated with the NACTAC interface system, each having its own unique function. The main control console (Fig. 8a), located in one bay of the antenna control console (Fig. 9), is used to input antenna commands to the computer in the digital mode. The displays available on this panel are

Antenna azimuth
Antenna elevation
GMT clock
Reverse clock
Time offset
Azimuth offset
Elevation offset
Local site range
Local site range rate
Remote site range
Remote site range rate
Mode display.

Also provided on the main control panel are groups of switches for data and command inputs associated with the control of the antenna in the digital mode. These switch groups are

Mode switches (designate az-el, program track, etc.)
Scan selection and initiation (spiral, elliptical, etc.)
Scan parameters (increment, amplitude, and rate)
Antenna angle designation and offsets
Display, cam, and acquisition control program selection
Local range and range-rate display
Remote range and range-rate display
Receiver selection.

None of the switches associated with this panel are hardware connected with the exception of the controls for the real-time clock. All commands for action are inputed to the computer by sensing switch conditions. After software interpretation, the computer then responds by performing the requested function, if valid, and setting the switch light.

The range and range-rate control switches are used to signal the computer to apply lamp power to the selected display and to select the proper quantity for display. The range and range-rate displays serve a dual purpose, to provide range information in Earth radii and range rate as monostatic doppler shift in Hz/GHz, or to display both the path loss as free space attenuation in dB between isotropic antennas and range rate in hertzes for a selected frequency.

The test controller's panel (Fig. 8b) is located in one bay of the test controller's console and is used to monitor the action of the antenna during an experiment. It is from this panel that the reverse clock and any desired computer control of the experiment being performed is activated. Displays available on this panel are identical to those on the main control panels described previously.

Control switches located on this panel are

Reverse clock preset, stop, and start
Local range and range-rate display
Remote range and range-rate display
Quick look initiation
Computer experiment control switches.

The range and range-rate switches on this panel perform functions identical to those on the main control panel.

The quick-look initiation switches allow the operator to obtain look angles for the object to be tracked without outputing to the line printer. This feature allows the operator to advance or decrease the selected time in operator-selected increments to determine present and future pointing angles, range, and range-rate corresponding to the orbital path of a desired object, the parameters of which have been entered into memory. All actions of these switches are subject to the antenna operation not being in digital mode.

The computer experiment control switches allow the operator to control the experiment via the computer once the appropriate software defining the action desired for each switch has been provided. This feature permits flexible use of the computer to perform or assist in experiments.

The computer control panel (Fig. 8c) is located in a desk console in close proximity to the computer's operating console (see Fig. 7b), and is used to monitor the operations taking place in the interface. Most function codes have an associated lamp located on this panel which provides the operator with a cursory view of internal operations. This panel is used mainly for trouble shooting, debugging, and monitoring general operations. Displays available on this panel are

Antenna azimuth
Antenna elevation
GMT clock
Reverse clock
Time offset
Azimuth offset
Elevation offset
Mode display.

The only switches associated with this panel are those for control of the GMT and variable clocks.

GENERAL INPUT-OUTPUT STRUCTURE

Function Codes

With the exception of the real-time clock described previously, all system operations are controlled by instructions from the computer. These instructions, known as function codes, are sent by the computer as 12-bit binary words plus control signals to the interface where the instructions are converted to octal form by a function decoder associated with each of the input-output channel groups (i.e., Channels 3 and 4, and Channels 5 and 6). The function codes perform one of three basic operations; selection, sensing, or action. Below is an example of one action code and how its components are arranged:

740	3	5200
Select	on this channel	this function

This function code, were it selected, would instruct the interface to interrogate the antenna azimuth digital encoder. Were the above instruction to have a 7 in place of the 0 in the select portion of the instruction (i.e., 747), the instruction would perform a sense operation as explained below.

Select codes are used to gate equipment or registers for the purposes of transmitting data or arming interrupts. The use of these codes allows a large number of inputs and outputs to be connected to the limited number of input/output (I/O) channels in the computer.

Sense codes are used to check the status of operations within the interface equipment or of equipment connected externally to it but under the control of the interface. They provide a measure of system monitoring when associated with the select and interrupt operations and some action functions.

Action codes are used to perform a function such as turning on lamp and relay power or individual displays, or to provide a relay closure to perform an operation which can be defined as the need arises. The closure is available to operate external equipment associated with the defined need.

All function codes are decoded and gated in an identical fashion for both I/O channel groups. A simplified logic presentation for the function decoder is given in Fig. 10. A 12-bit register in the computer is available for each I/O group, and each channel in a group has a control signal associated with it. The input channel signal is referred to as the Input Function Ready (IFR) signal. The output channel signal is referred to as the Output Function Ready (OFR) signal. The lower 12 bits in the operand (base execution address) of the instruction being executed (see Fig. 4) are placed in the 12-bit register, and the upper 3 bits of the operand are used to determine which I/O group register is used and which function ready signal is sent to the interface equipment. The function

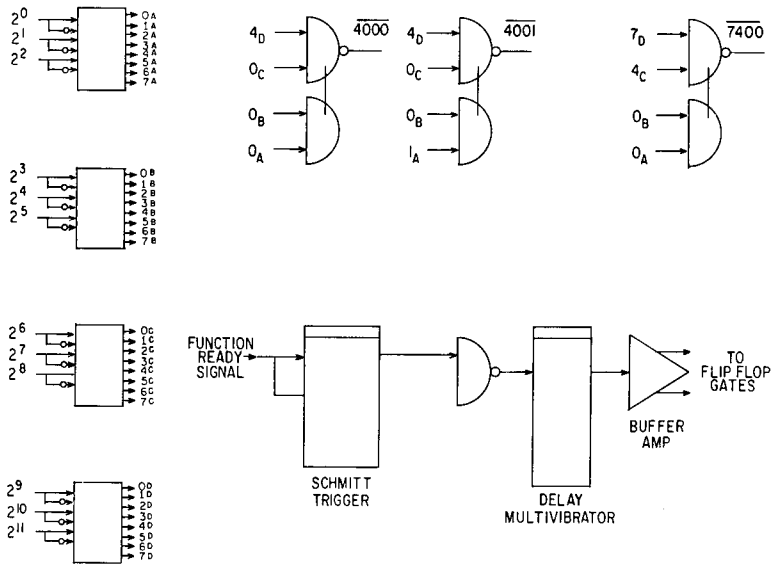

Fig. 10 - Simplified function decoder logic

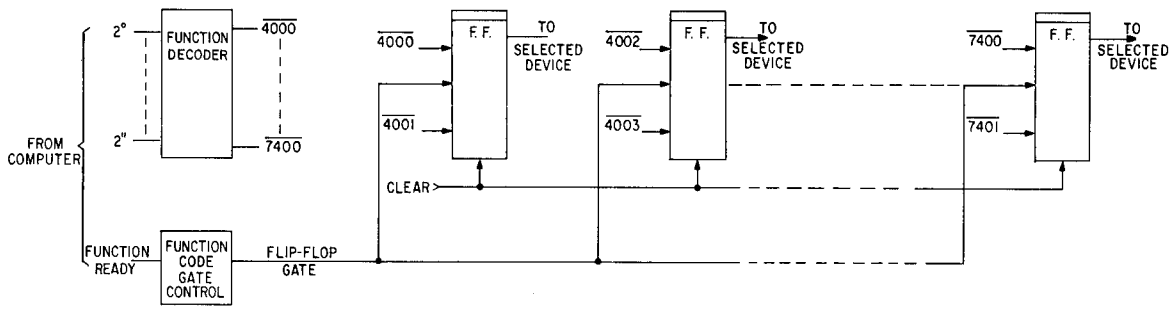

Fig. 11 - Simplified function - code selection logic

ready signal is sent by the computer to the interface where it is shaped and buffered and used as a gate or clock signal for all the select and action flip-flops associated with the given channel. The only flip-flop which is set is the one for which there is a signal at the output of the decoder. Figure 11 is a simplified block diagram of the function code-selection logic.

The sense operation is an exception to the above. While the selection of the proper 12-bit register is the same, there is no function ready pulse generated by the computer. Instead, a sense ready signal is sent to the appropriate channel. This signal is used to gate the logical AND of the function code and the event being sensed, in order to create a sense response signal to the computer. The state of the sense response signal determines which action the computer will take.

There are also provisions in the interface equipment to interrupt the computer's normal sequence on the occurrence of a predetermined event. An interrupt signal is produced by the logical AND of a select code and the occurrence of an event, be it the setting of a flip-flop or a pulse from an external device. Each code is used to interrupt on a different condition and immediately signals the computer that the preselected event

has occurred. The interrupt codes are identical to select codes, the interrupt to the computer being generated by circuitry in the interface equipment. The interrupt action is as follows: On selection of an interrupt code the selection flip-flop associated with it is set. The output of this selection flip-flop is used to arm an interrupt signal flip-flop. No action takes place until a signal is received from the associated hardware, whereupon the signal flip-flop is clocked by the interrupt signal and this flip-flop is set. The interrupt flip-flops are then connected to produce the logical OR of all interrupts in each channel. If an event for which the computer has made an interrupt selection occurs, a signal from the OR circuitry is sent to the computer via the appropriate channel interrupt line. The computer then enters an interrupt sequence to process the interrupt.

In order to determine which interrupt has occurred, the interface system has been designed to include a sense code for each of the interrupt codes. These sense codes use the same operand as the interrupt they are sensing, and, when selected, these codes sense the condition of the interrupt signal flip-flop. If the interrupt has occurred, a signal is sent to the computer as a sense response and the computer responds accordingly. As an example: If the sense code 74 7 34000 were to be selected, the interface would sense the condition of the equipment associated with the 74 0 34000 function code which happens to be the interrupt or sample time. If the interrupt had occurred the interface logic would return a sense response to the computer which would cause the computer to execute a jump instruction to its present memory location plus two (SKIP EXIT). If no response is received, the computer merely executes a jump to the next instruction.

In addition, the interface is equipped with function codes to sense the inverse of any operation so as to provide a response if no action has occurred. In the case previously described, the appropriate sense code would be 74 7 34001.

Each operation which may cause an interrupt to the computer may be sensed in lieu of causing an interrupt by selecting any of another series of sense codes provided for this purpose.

For the most part, interrupts are fixed and defined; however, there are several interrupt inputs provided by patching, which are not defined and which are used to interrupt from a source external to the interface.

All external function codes currently used in the interface equipment are listed in Appendix B, along with their functions.

Registers

The interface logic will operate at a speed faster than that of the computer, which has permitted the design of registers for buffering to be relatively free of timing problems for many operations. Many of the registers, particularly those which are used to buffer information to or from equipment within the interface itself, can be buffered at a rate determined only by the computer's maximum data rate. The buffering operation is controlled by an exchange of control signals between the computer and the interface equipment.

There are some operations performed by the interface involving external equipment such as an A/D converter, which are not capable of operating at data rates as fast as that of the interface itself. Registers and control logic associated with these operations are configured so as to permit a response input from the equipment to alert the interface to its condition or acknowledge its receipt of information. In the use of this type of equipment, the timing is controlled only by the speed of the device and upon receipt of a signal from the external equipment, buffering is resumed.

The I/O timing waveforms for the computer-interface buffer are shown in Appendix C.

There are three types of gated registers used in the interface equipment: scan, alternating, and single action. All three types can be found in each of the I/O channels of the interface and are of both flip-flop and gate configuration. These registers, when selected, clear out any previously selected I/O registers so that the information is transmitted to the correct register. For this reason, they usually must be selected each time the particular register is required unless no other register has been selected since buffering was last terminated.

The single-action registers are 24-bit registers generally used to transfer information between the computer and equipment external to the interface equipment. An exception are three single-action registers associated with presetting the reverse clock and entering reverse clock time information to the computer. The external equipment which can be controlled by these registers are possibly a slaved antenna, digital resolver (D/R), and several spares which have not as yet been assigned.

Alternating registers in the interface select and gate two separate holding registers alternately as the data buffer advances and respond immediately to the buffer, requiring no signalling from the equipment which they control. The buffer may start on either of the two register outputs by using the proper function codes associated with them. These registers are generally associated with transferring such data as antenna azimuth and elevation angles or terminal frequency.

Scanning registers are also available in the system which allow either the transfer of one word in a block, a portion of a block, or a full block of data. The scanners gate individual fixed-purpose holding registers and addressable registers and control the channel selection in external equipment such as multichannel digital-to-analog converters. Scanning registers range in size from a block of six registers in a scanner used in the antenna control I/O channels to a block of 160 used in the data acquisition/display channels. Several scanners, particularly those scanners associated with console switch and internal clock inputs to the computer, as well as console displays, are not cyclic nor are they presettable and are usually buffered as a block. Recycling scanners which are generally associated with conversion equipment and a 160-channel multiplexer located in the interface equipment allow parallel entry and therefore may be preset to any position in the scanner.

All registers which are connected to external equipment requiring that a response or ready signal be sent to the interface are of the single-action, or scanning type.

CHANNELS 3 AND 4, ANTENNA CONTROL

Function Codes

All operations in Channels 3 and 4 are controlled by function codes as discussed previously. Action codes are used to turn lamp and relay power and individual displays on or off and to perform functions external to the interface through the use of relay closures. All displays associated with the antenna and its control are activated by Channel 4 action codes, whereas action codes associated with Channel 3 perform functions external to the interface system such as antenna operating-mode change, receiver selection, and transfer of computer peripheral equipment from one I/O channel group to another.

To permit the operator to clear functions associated with the interface, each channel is provided with function codes to provide entire channel, entire group, or individual selection clearing.

Associated with each channel are one action code which is used to clear all channel operations including action, selection, and interrupt functions, and several group clearing function codes used to clear an entire group of selections such as all interrupt selections, all interrupt signals, or all action codes. There is also a function code associated with each action code, each interrupt selection, and each interrupt signal flip-flop to remove the individual selection or signal.

Each channel has eight interrupt functions associated with it. These codes are used to interrupt the normal program routine of the computer as mentioned previously, and force it to branch to a subroutine to ascertain the reason for the interrupt and to perform a function associated with the occurrence of the event that generated the interrupt. Interrupt inputs in the Channel 3 equipment are provided for external equipment signals such as azimuth and elevation encoder ready signals, and several unique interrupts which are used solely for software level changes. Two of these unique interrupts are the sample interrupt and the subsample interrupt. These interrupts are clock pulses which interrupt the computer at intervals set by a special patching arrangement which has been included to allow interrupt pulses ranging from 1 to 512 pps. The present patching arrangement is for a 16-pps sample interrupt for sampling console inputs, updating displays, and forming antenna commands, and a 128-pps subsample interrupt for interrogating and sampling the digital encoder output and for generating antenna servo errors. Also associated with Channel 3 is a forced interrupt and a strobe interrupt, both of which are used primarily for the control of software level changes. The forced interrupt creates an interrupt immediately after it is selected, while the strobe interrupt is set to interrupt 128 times/sec by the aforementioned patching.

Channel 4 interrupts include signals to alert the computer that the tracking receiver is above track threshold, that the reverse clock has counted down to zero, and spare external inputs which are available for the use of external equipment interrupt inputs.

For every interrupt code in Channels 3 and 4 there is a sense code to determine the source of the interrupt.

Special Inputs (Channel 3)

All antenna position and status inputs are inputed to the computer through Channel 3 interface logic, as are all antenna commands while in the digital mode. These inputs are both switch and logic inputs and are inputed to the computer on Channel 3. All inputs on this channel are inserted through the interface input data unit, Fig. 12, which is a 24-bit, multi-input matrix register consisting of 20 two-input NAND gates for each bit. All of the NAND gates are wired in an OR configuration for each of the 24 input bits to the computer. One input to each gate is an information input, and the other input is a gating or clock input signal which is armed by the individual register flip-flop and gated by input timing logic. This gating input is common to all 24 bits to form an individual input register. There are thus 20 individual input registers, each of which is controlled by a different selection code or position in a scanner. The assigned inputs to the registers are

Antenna azimuth
Antenna elevation
Optical azimuth
Optical elevation
Slave
System Status 1
System Status 2
System Status 3
Time

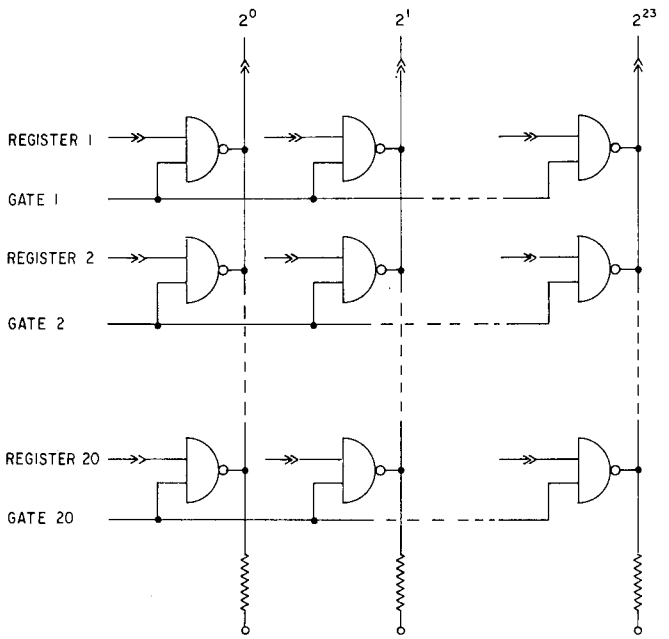

Fig. 12 - Simplified input data unit

Time Offset
Azimuth Designate
Elevation Designate
Vector Velocity Designate
Scan Parameters
Spare A
Spare B
Spare C
Reverse Clock Input
Reverse Clock Preset
Digital Resolver (not presently used).

As a single-action, alternating, or scanning register is selected and advanced, the output of the register is used to gate the input register associated with it, thus placing the information on the computer data lines to be stored in memory.

All parameter inputs from the operator such as position designations, scan parameters, offsets, and reverse clock preset are inputed via thumbwheel switches located on both the main control console and the test controller's console panels (see Fig. 8a and 8b). These switches are of the maintained-action type with a BCD code input to the interface for each digit.

All commands for action, displays, or control of inputs are by momentary-action switches located on the same consoles as the parameter inputs. These switches are sensed every sampling period, and action is taken and continues until removed by depressing one of the clearing switches or by commanding a conflicting operation such as changing from such modes of digital control as Program Track to Designate Az-El. All momentary-action and thumbwheel switches are inputed in a block controlled by an acyclic 12-word scanner which is generally inputed as a 12-word block. Also inputed on this block is the status of the antenna mode-control switches associated with the antenna servo circuitry.

Antenna azimuth and elevation angles are entered into the computer through use of an alternating register. The digital outputs of the antenna's azimuth and elevation digital encoders are each connected to one of the input data unit registers.

Channel 3 is also equipped with several spare 24-bit input registers. Access to these registers is available at connectors located in the rear of the interface equipment.

Special Outputs (Channel 4)

Channel 4 is used to output information to displays, to control terminal frequencies, and to output digital tracking errors to a 6-channel, 12-bit D/A converter which generates the analog error voltage used to drive the antenna servo in the digital mode.

All Channel 4 outputs are through the Output Data Unit located in the interface equipment. This unit consists of 24 data lines from the computer which are used to generate 24 assertion and 24 negation data lines. Each assertion and negation bit is then common to the appropriate bit of a 17- by 24-bit matrix flip-flop register having column addressing. These lines are also common to the antenna error D/A converter and reverse clock preset registers which are in turn gated by scanning and single-action registers, respectively. Each of the 17 output registers (columns) is gated by a single, alternating, or scanning register output. Information gated into any of the 17 output registers is stored in the flip-flop, the outputs of which are either decoded to drive displays or are used directly to drive lamps or relays.

The reverse clock requires no storage other than that inherent in the flip-flop nature of its construction. For this reason, the 24 data lines are brought directly into the reverse clock to provide parallel drop-in when the proper function code is selected. The D/A converter associated with the antenna servo also contains its own register and is therefore connected in the same fashion as the reverse clock.

All information displays are of the in-line projection type. The outputs of the storage registers are decoded to provide a decimal output which is used to drive the displays through lamp drivers. All lamps associated with the momentary action switches are driven directly by the outputs of three registers through lamp drivers. Power for all displays is controlled by function codes which operate relays in the interface which in turn apply power to the display and switch lamps.

Digital control of the antenna servo is accomplished by computing an error angle from the antenna command position and the present antenna position and outputing this error angle in the proper format to a D/A converter located in the interface system expressly for this purpose. By selecting a channel in the converter through a scanning register in the interface, the information located in the upper 12 bits of the computer data lines is set into the converter channel selected, and an analog voltage is obtained at the output which is in turn used as an error signal in the azimuth or elevation servo.

Control of the telescope cine camera located behind the dish can be accomplished through the digital system. The shutter may be activated to take a single frame, single frame time exposure, or operate in cine mode. The shutter status may also be sensed.

CHANNELS 5 AND 6 DATA ACQUISITION AND DISPLAY

Function Codes

As is the case with equipment associated with I/O Channels 3 and 4, all equipment connected to Channels 5 and 6 is controlled by the use of function codes. These are

available to select the channel address of the multiplexer and the mode of data transfer for Channel 5, and to select the D/A converter channel and mode of data transfer for Channel 6. One select code is provided in each channel to select a digital I/O register for transferring digital data.

In addition, four select codes are available in each channel for interrupt functions. Channel 5 interrupts include an interrupt on a clock pulse from the variable clock and an interrupt for an excessive clock rate for data acquisition. The remaining Channel 5 interrupt select codes are available for external equipment and have no fixed assignment. One Channel 6 interrupt is available to provide an interrupt for a clock rate which is faster than the rates at which the external equipment may operate. The remaining Channel 6 interrupts are also available for external equipment as in Channel 5.

Action codes are provided on Channels 5 and 6 to clear all channel operations, remove all interrupt selections, remove interrupt selections individually, clear all interrupt signal flip-flops, and clear individual interrupt signal flip-flops. Channel 5 action codes are also provided for selecting any of the dc calibration voltages, for setting the variable clock rate to the setting on thumbwheel switches provided for this purpose, and to turn the variable clock on and off.

Sense codes corresponding to interrupt functions in each channel are provided to sense the status of each channel interrupt to determine which interrupt has occurred. Also provided are sense codes to the check status of channel equipment in lieu of causing an interrupt.

Channels 5 and 6 are used almost exclusively for the purpose of inputing and outputing analog data, and for this reason the interface structure is necessarily special. Channel 5 conversion equipment consists of a 160-channel, randomly addressable multiplexer, and a 12-bit A/D converter. The multiplexer channel may be selected by software through the interface, or each channel may be selected manually by use of thumbwheel switches located on the front panel of the instrument. Manual operation, however, is used only for test purposes. The full-scale range of the A/D converter may be varied in three steps (± 2.5 V, ± 5 V, and ± 10 V) through use of a switch provided for this purpose on the front panel of the instrument. In the process of channel selection, sampling, and conversion, the effective through-put of the multiplexer and A/D converter is slower than that of the computer data transfer rate. For this reason an external signal from the A/D converter is used to inform the computer of the completion of a sample and thereby controls the effective data transfer rate.

Variable Clock

Common to both channels is a variable clock provided for clocked data conversion. The clock rate, which may be selected by use of the function code 74 0 570mn, is determined by the equation $C = F\ 10^m/(n + 1)$ pps, where F is an integer from 1 to 9 representing the input frequency, C is the clock rate in pulses per second (pps), and m and n have integral values. Nine input frequencies F, from 100 to 900 kHz in 100-kHz steps, are available from a precision frequency standard by patching. Division is accomplished by using m to select decade counters to accomplish a division in decade steps from 10^0 to 10^5. For this case, m may assume a numerical value from 0 to 5. The output of the decade counters may be divided by a value from 1 to 8 by use of n. This divisor is then equal to n + 1. When the m = 6 the output of the variable clock is equal to $16/(n + 1)$ pps to relate the variable clock to the 16-pps system rate. When m = 7, any external signal which does not exceed 1 MHz and is sine wave in nature may be used to provide an output = external source/(n + 1) pps. The m and n values described above may be entered through thumbwheel switches located on the NACTAC computer control console by either selecting a function code which will set the clock rate to the switch setting or depressing the "ENTER m n" momentary action switch.

The clock may be started and stopped by either a function code or a manual push-button; starting may be immediate or on the next second tick from the system GMT clock.

Channel 5 Input-Output Structure

To permit the selection of any channel or group of channels in the multiplexer, special registers have been included in the Channel 5 interface structure. These registers are briefly described below.

U Register. This register receives and stores the channel address of the multiplexer desired as the starting point of conversion. The maximum count of this register is 237 octal.

V Register. This register receives the starting address from the U register and transfers the address to the multiplexer. If more than one channel is to be converted, this register is incremented after each conversion. Total count of this register is identical to that for the U register.

S Register. For purposes of clocked data transfer, the S register has been provided. This register receives the decimal number of channels to be converted per clock pulse. The total count of the S register is 2^8 -1.

T Register. This register receives the information stored in the S register on each clock pulse. As each channel in the multiplexer is sampled the T register decrements until T = 0. Conversion then stops until the next clock pulse.

The operational aspects of Channel 5 which are described below are presented in block diagram form in Fig. 13.

There are four data transfer modes in Channel 5. Three of these modes are associated with the analog conversion circuitry. Mode 1 is selected by the 74 0 55mnp function code. When this mode is selected, the channel address, determined by the mnp of the function code, is stored in the U register and gated into the V register. This register is connected through buffers to the multiplexer which uses these eight bits to select the proper channel when the computer data buffer (buffer active) is activated. The proper channel is selected only after an "address set" pulse is received from the interface.

As each multiplexer channel is sampled, the V register is incremented to advance the multiplexer channel. This action continues until the computer data buffer is dropped. As each multiplexer channel is selected the associated analog signal is connected to the A/D converter. After receiving a signal from the multiplexer that the proper channel is connected (convert enable), the conversion process begins. After the conversion has been completed, the digital output is placed in the upper 12 bits of a 24-bit input register, and the address of the channel being converted is received from the multiplexer on separate lines and placed in the lower eight of the remaining 12 bits in the register.

The A/D converter then signals the computer (A/D Ready) through the interface that the conversion process is complete (input data ready), and the computer accepts the 24-bit data word. If more than one channel is to be sampled, the computer causes the multiplexer channel to be advanced via buffer resume and increment V and the process is continued until all the channels to be sampled are converted.

Mode 2 is a sequential mode controlled by the function code 74 0 55, m+4, np. In this mode, the lower eight bits (m+4, np) are placed in the U register as for the previous mode, and the address is then gated into the V register. The same action as was described for

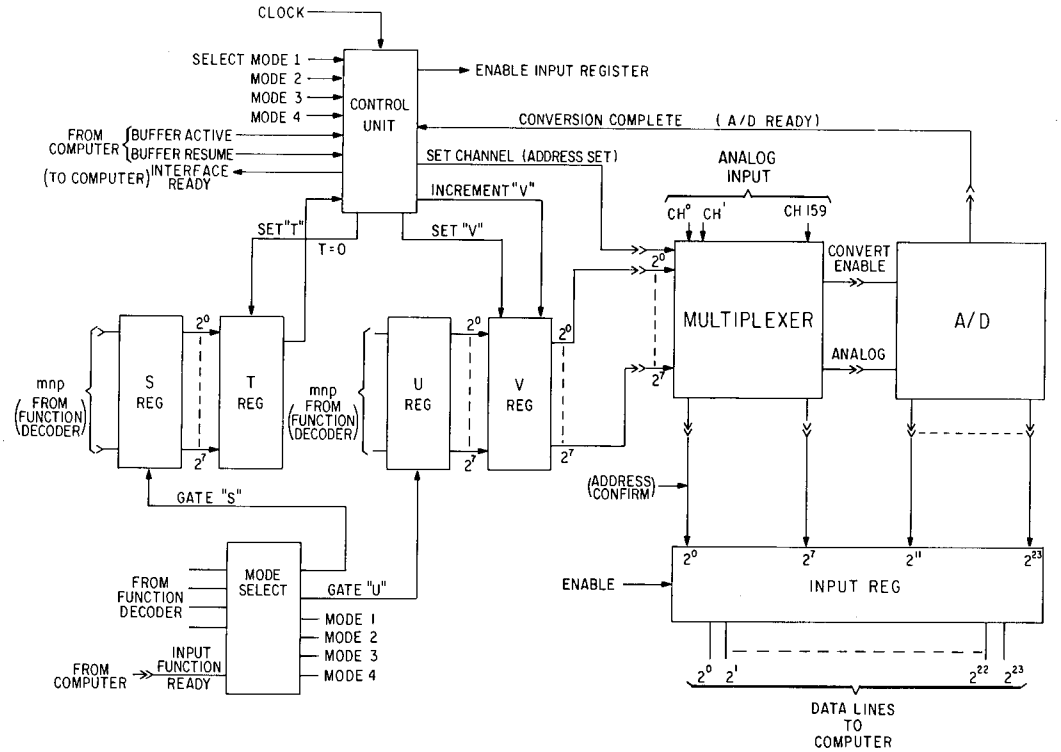

Fig. 13 - Functional block diagram of Channel 5 data transfer logic

74 0 55mnp mode holds true for Mode 2 except that if no new selection has been made and the buffer is reactivated, the next sequential channel following the last one sampled in the previous block will be converted.

To allow clocked data transfer, the third operating mode (Mode 3) for Channel 5 has been provided. This mode is unique in that it requires that two function codes be selected. The first code selected must be the group length function code 74 0 56, m+4, np. This code determines the number of channels sampled in one clock period. Selection of this code places the mnp of the instruction into the S register. The mode-selection function code 74 0 56, mnp enters the mnp of the instruction into the U register, as described previously. When the contents of the U register are gated into the V register, the contents of the S register are also gated into the T register.

No data are converted upon channel activation until a clock pulse is received. Upon receiving the clock pulse, the multiplexer is set to the channel selected by the V register (address set) and the conversion process begins at free cycle rates until the block determined by the T register is converted, whereupon the process is halted (T = 0) until the next clock pulse.

If the clock rate selected is too high a frequency, such that a clock pulse occurs during the free-cycle transfer, the data transfer is not aborted. Instead, a signal is available through interrupt and sense flip-flops to alert the computer to this condition. After the data transfer has advanced through the T register count, it will not continue until still another clock pulse is received. This provision was incorporated to allow the complete block of data to be transferred as a block and to allow software to recognize that the data are not taken at the specified clock rate.

The fourth mode of operation for Channel 5 is the same as the single-action register operation described for Channel 3. This 24-bit register is a spare input register and may be used to input 24 bits of digital data to the computer. Control circuitry for this register must be supplied by the input device.

Channel 6 Input-Output Structure

Like Channel 5, this channel has four modes of operation controlled by function codes. The first mode is a free-cycle transfer mode in which the data rate depends only on the external 6-channel, 12-bit D/A converter. The upper 12 bits of the output word from the computer contain the digital data to be converted. The lower 12 bits may contain the D/A channel number. The selection code for the mode 74 0 6500n determines which channel is to be used in the conversion process when n = 0 to 5. Figure 14 is a simplified block diagram of the Channel 6 operation.

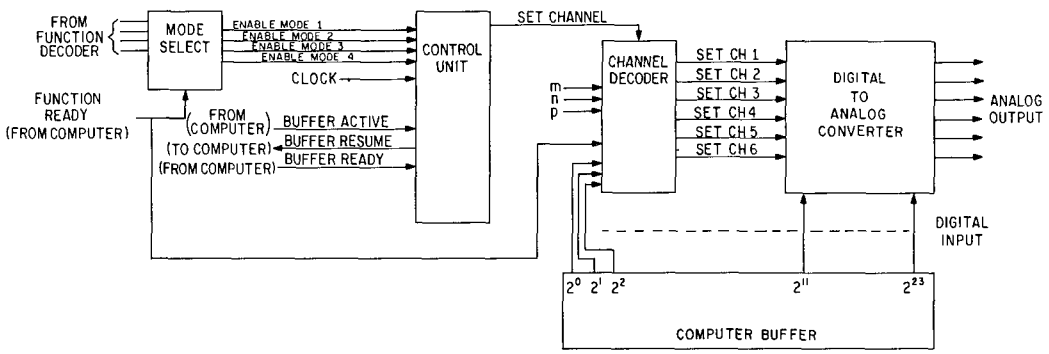

Fig. 14 - Functional block diagram of Channel 6 data transfer logic

The three bits of the function code corresponding to n (three least significant bits) are connected to a three-stage register. The outputs of the register are connected to an octal decoder which decodes the binary output of the register. No output is received from the decoder until the channel is activated. Upon channel activation the computer places the data to be outputed on the 24 data lines. The channel decoder then enables the channel set line selected, and the data on the highest-order 12 bits of the output word are then converted by the selected channel.

The desired channel may be selected by software as well. If in the function code n = 6 or 7, the output of the first octal decoder is used to strobe a second decoder. The desired channel number is placed in binary form in the three least significant bits of the output word from the computer, which are connected to the second decoder. The output lines (0 to 5) of the second decoder are connected in OR fashion with those of the first decoder to provide the channel set pulse.

The second operating mode for Channel 6 (74 0 6510n) is identical to the first mode except that the variable clock is used to transfer one word on each clock pulse.

The third operating mode (74 0 6520n) is identical to the second mode except that on each clock pulse two successive words are transferred. For this, code n may take on the octal value 0, 2, 4, 6. For n = 0 to 4, n is used to select the desired channel as for 74 6500n mode. For n = 6 the three least significant bits of the data word are used.

The channels are always selected in pairs such as 1 and 2, 3 and 4, or 5 and 6, and are selected odd channel first. If n takes on the values 1, 3, 5, or 7, n will be converted back to 0, 2, 4, or 6 internally.

The fourth operating mode for Channel 6 (74 0 67400), a single-action mode, allows the output of a 24-bit digital data word to an external device. All control circuitry for control of buffering, including a response signal, must be included in the device.

Uses of Channels 5 and 6

The uses for Channels 5 and 6 are varied. Any analog input within scaling ranges of the A/D converter may be inputed. Provision has been included for the termination of special, low-noise, analog data lines in close proximity to the conversion equipment. In addition, variable-cutoff-frequency signal-processing differential amplifiers with five-pole Butterworth filters are available through patching for the effective reduction of common mode problems caused by different grounding systems. The opposite ends of these data lines terminate at various points in the receiver system on patch panels. This will allow the input of receiver signal noise and frequency data, as well as the input of signals from electromechanical devices such as synchros, resolvers, weather measuring devices, etc. Channel 6 analog outputs may be used to drive an x-y plotter and an x-y oscilloscope, both of which are available as a permanent part of the system.

CONCLUSION

The computer system associated with the Waldorf facility is fully capable of providing the control of operations associated with an experiment, including pointing, scanning, and control of r-f sections of the antenna system. It is also capable of displaying all antenna parameters for operator use. This system, while providing direct control over all commands to the antenna through the antenna control panel switches, gives the operator a sense of control which could not be realized by direct computer entry.

The interface system has built-in provisions for expansion and, in many cases, spare controls and registers are already available for use. This permits use of the computer to control not only the antenna system at the Waldorf facility but remote antennas as well. The use of this provision would allow the central control of experiments being conducted by both antennas. In addition, the system has built-in provisions for data acquisition and display which enhance its use as a tool for experimentation.

Appendix A

CDC 924A INSTRUCTION REPERTOIRE

ADD	Add
ADL	Add Logical
AJP	A Jump
ALS	A Left Shift
ARS	A Right Shift
ATI	A to Index
CMA	Complement A
CMQ	Complement Q
DVI	Divide
ENA	Enter A
ENI	Enter Index
ENQ	Enter Q
EQS	Equality Search
EXF	External Function
IJP	Index Jump
INA	Increase A
INI	Increase Index
INQ	Increase Q
IOL	Input/Output Lockout
ISK	Index Skip
LAC	Load A Complement
LDA	Load A
LDL	Load Logical
LDQ	Load Q
LIL	Load Index
LLS	AQ Left Shift
LQC	Load Q Complement
LRS	AQ Right Shift
MEQ	Masked Equality
MTH	Masked Threshold
MUI	Multiply
PTS	Pattern Search
QJP	Q Jump
QLS	Q Left Shift
QRS	Q Right Shift
QTI	Q to Index
RAD	Replace Add
RAO	Replace Add One
RSB	Replace Subtract
RSO	Replace Subtract One
SAL	Substitute Address
SBL	Subtract Logical
SCA	Scale A
SCL	Selective Clear
SCM	Selective Complement
SCQ	Scale AQ
SIL	Store Index
SKH	Skip High
SKL	Skip Low
SLJ	Selective Jump
SLS	Selective Stop
SSH	Storage Shift
SSK	Storage Skip
SST	Selective Set
SSU	Selective Substitute
STA	Store A
STL	Store Logical
STQ	Store Q
SUB	Subtract
TAL	Tally
THS	Threshold Search
UJP	Unconditional Jump
URJ	Unconditional Return Jump
WCI	Wait Channel Inactive
XAQ	Interchange A and Q
XEC	Execute

Appendix B

INTERFACE SELECT CODES

FUNCTION SELECT CODES FOR CHANNEL 3

74 0 30000 Master clear - clears all Channel 3 equipment and interrupt selections, clears all interrupt signals, and sets appropriate clear and zero indications.

74 0 34000 Interrupt on sample time
4001 Remove interrupt selection above
4002 Interrupt on subsample time
4003 Remove interrupt selection above
4004 Interrupt on azimuth angle ready
4005 Remove interrupt selection above
4006 Interrupt on elevation angle ready
4007 Remove interrupt selection above
4010 Interrupt on both azimuth and elevation ready
4011 Remove interrupt selection above
4012 Interrupt on digital resolver (D/R) ready to input
4013 Remove interrupt selection above
4014 Forced interrupt
4015 Remove interrupt selection above
4016 Interrupt on strobe pulse
4017 Remove interrupt selection above

Logical AND of antenna 1 and antenna 2 ready signals. If either antenna 1 or antenna 2 is disconnected, the other functions alone.

74 0 34100 Remove all interrupt selections above

74 0 34200 Clear interrupt signal for sample time
4201 Clear interrupt signal for subsample time
4202 Clear interrupt signal for azimuth ready
4203 Clear interrupt signal for elevation ready
4204 Clear interrupt signal for both azimuth and elevation ready
4205 Clear interrupt signal for D/R ready to input
4206 Clear interrupt signal for forced interrupt
4207 Clear interrupt signal for strobe pulse

74 0 34300 Clear all interrupt signals

74 0 35000 Initiate synchro-slaved mode
5001 Terminate synchro-slaved mode
5002 Initiate auto-track mode
5003 Terminate auto-track mode
5004 Initiate rate memory
5005 Terminate rate memory
5006 Receiver program select
5007 Receiver external select

74 0 35010 Select receiver No. 1 tracking errors
5011 Select receiver No. 2 tracking errors
5012 Initiate operation Op 1
5013 Terminate operation Op 1

5014 Magnetic tapes Channel 5 and 6 operation
5015 Magnetic tapes Channel 3 and 4 operation
5016 Line printer Channel 1 and 2 operation
5017 Line printer Channel 5 and 6 operation

74 0 35100 Terminate all above operations

74 0 35200 Interrogate antenna azimuth digital encoders
5201 Interrogate antenna elevation digital encoders
5202 Interrogate antenna both azimuth and elevation digital encoders

74 0 35300 Select antenna 1 azimuth, then elevation encoder
5301 Select antenna 1 elevation, then azimuth encoder

74 0 35400 Select antenna 2 azimuth, then elevation encoder
5401 Select antenna 2 elevation, then azimuth encoder

74 0 35500 Select slave-in

74 0 35600 Select block of:
system status No. 1
system status No. 2
system status No. 3
real-time clock
time offset
azimuth designate - offset
elevation designate - offset
velocity designate
scan parameters
spare B
spare C
spare D

74 0 35700 Select reverse clock
5701 Select test controller console reverse clock preset

74 0 36000 Select D/R

FUNCTION SELECT CODES FOR CHANNEL 4

74 0 40000 Master clear - clears all Channel 4 equipment and interrupt selections, clears all interrupt signals, and sets appropriate clear and zero indications.

74 0 44000 Interrupt on receiver No. 1 above track threshold (enable)
4001 Remove interrupt selection above (defeat)
4002 Interrupt on receiver No. 2 above track threshold (enable)
4003 Remove interrupt selection above (defeat)
4004 Interrupt on reverse clock all zeros
4005 Remove interrupt selection above
4006 Interrupt on slave out request (OC1)
4007 Remove interrupt selection above
4010 Interrupt on output condition 2 (OC2)
4011 Remove interrupt selection above
4012 Interrupt on output condition 3 (OC3)
4013 Remove interrupt selection above
4014 Interrupt on output condition 4 (OC4) (Program Timing No. 1)

4015 Remove interrupt selection above (Program Timing No. 1)
4016 Interrupt on output condition 5 (OC5) (Program Timing No. 2)
4017 Remove interrupt selection above (Program Timing No. 2)

74 0 44100 Remove all interrupt selections above

74 0 44200 Clear interrupt signal for receiver No. 1 above track threshold
4201 Clear interrupt signal for receiver No. 2 above track threshold
4202 Clear interrupt signal for reverse clock all zeros
4203 Clear interrupt signal for slave out request (OC1)
4204 Clear interrupt signal for OC2
4205 Clear interrupt signal for OC3
4206 Clear interrupt signal for OC4
4207 Clear interrupt signal for OC5

74 0 44300 Clear all interrupt signals

74 0 45000 Turn on main lamp and relay power
5001 Turn off main lamp and relay power
5002 Turn on azimuth-elevation displays
5003 Turn off azimuth-elevation displays
5004 Turn on local range, range-rate displays
5005 Turn off local range, range-rate displays
5006 Turn on remote range, range-rate displays
5007 Turn off remote range, range-rate displays

74 0 45010 Turn on reverse clock display
5011 Turn off reverse clock display
5012 Turn on azimuth offset displays
5013 Turn off azimuth offset displays
5014 Turn on elevation offset displays
5015 Turn off elevation offset displays
5016 Turn on time offset displays
5017 Turn off time offset displays

74 0 45100 Terminate all above operations

74 0 45200 Select spare register

74 0 45300 Select frequency control No. 1, No. 2
5301 Select frequency control No. 2, No. 1

74 0 45400 Select spare 1, then spare 2
5401 Select spare 2, then spare 1

74 0 45500 Select slave out

74 0 45600 Select block of:

computer status No. 1	azimuth offset
computer status No. 2	elevation offset
computer status No. 3	range No. 1
antenna azimuth	range-rate No. 1
antenna elevation	range No. 2
time offset	range-rate No. 2

74 0 45700 Stop and reset reverse clock and select preset
5701 Start reverse clock
5702 Stop reverse clock

74 0 4600n Select cyclic D/A block starting at D/A channel n+1; $0 \leq n \leq 5$ (antenna error, D/A channels 1 and 2 for az and el)

74 0 46100 Take one frame on Flight Research camera

SENSE CODES FOR CHANNEL 3

74 7 34000 Skip exit on interrupt for sample time
4001 Skip exit on no interrupt for sample time
4002 Skip exit on interrupt for subsample time
4003 Skip exit on no interrupt for subsample time
4004 Skip exit on interrupt for subsample time
4005 Skip exit on no interrupt for subsample time
4006 Skip exit on interrupt for elevation angle ready
4007 Skip exit on no interrupt for elevation angle ready
4010 Skip exit on interrupt for both azimuth and elevation ready
4011 Skip exit on no interrupt for both azimuth and elevation ready
4012 Skip exit on interrupt for D/R ready to input
4013 Skip exit on no interrupt for D/R ready to input
4014 Skip exit on forced interrupt
4015 Skip exit on no forced interrupt
4016 Skip exit on interrupt for strobe pulse
4017 Skip exit on no interrupt for strobe pulse

74 7 35000 Skip exit on sample time true
5001 Skip exit on sample time false
5002 Skip exit on subsample time true
5003 Skip exit on subsample time false
5004 Skip exit on azimuth angle held in register
5005 Skip exit on azimuth angle being digitized
5006 Skip exit on elevation angle held in register
5007 Skip exit on elevation angle being digitized
5010 Skip exit on azimuth and elevation angles held in registers
5011 Skip exit on azimuth and elevation angles being digitized
5012 Skip exit on D/R inactive
5013 Skip exit on D/R active
5014 Skip exit on slave input ready (IC1)
5015 Skip exit on slave input not ready (IC1)
5016 Skip exit on condition strobe pulse true
5017 Skip exit on condition no strobe pulse

SENSE CODES FOR CHANNEL 4

74 7 44000 Skip exit on interrupt for receiver No. 1 above track threshold
4001 Skip exit on no interrupt for receiver No. 1 above track threshold
4002 Skip exit on interrupt for receiver No. 2 above track threshold
4003 Skip exit on no interrupt for receiver No. 2 above track threshold
4004 Skip exit on interrupt for reverse clock all zeros
4005 Skip exit on no interrupt for reverse clock all zeros
4006 Skip exit on interrupt for slave out request (OC1)

4007 Skip exit on no interrupt for slave out request (OC1)
4010 Skip exit on interrupt for OC2
4011 Skip exit on no interrupt for OC2
4012 Skip exit on interrupt for OC3
4013 Skip exit on no interrupt for OC3
4014 Skip exit on interrupt for OC4
4015 Skip exit on no interrupt for OC4
4016 Skip exit on interrupt for OC5
4017 Skip exit on no interrupt for OC5

74 7 45000 Skip exit for receiver No. 1 above track threshold
5001 Skip exit for receiver No. 1 below track threshold
5002 Skip exit for receiver No. 2 above track threshold
5003 Skip exit for receiver No. 2 below track threshold
5004 Skip exit for reverse clock all zeros
5005 Skip exit for reverse clock not all zeros
5006 Skip exit for slave out request (OC1) true
5007 Skip exit for slave out request (OC1) false
5010 Skip exit for OC2 true
5011 Skip exit for OC2 false
5012 Skip exit for OC3 true
5013 Skip exit for OC3 false
5014 Skip exit for OC4 true
5015 Skip exit for OC4 false
5016 Skip exit for OC5 true
5017 Skip exit for OC5 false

74 7 45300 Skip exit for camera single-frame mode
5301 Skip exit for camera not single-frame mode

74 7 45400 Skip exit for camera open-shutter mode
5401 Skip exit for camera not open-shutter mode

74 7 46000 Skip exit for camera shutter open
6001 Skip exit for camera shutter closed

FUNCTION SELECT CODES FOR CHANNEL 5

74 0 50000 Master clear - clears all Channel 5 equipment and interrupt selections, clears all interrupt signals, and sets appropriate clear and zero indications.

74 0 54000 Interrupt on clock pulse
4001 Remove interrupt selection above
4002 Interrupt on clock rate excessive for 74056 mnp
4003 Remove interrupt selection above
4004 Interrupt on input condition 1 (IC1)
4005 Remove interrupt selection above
4006 Interrupt on input condition 2 (IC2)
4007 Remove interrupt selection above

74 0 54100 Remove all interrupt selections

74 0 54200 Clear interrupt for clock pulse
4201 Clear interrupt for clock rate excessive
4202 Clear interrupt for IC1
4203 Clear interrupt for IC2

74 0 54300 Clear all interrupts

74 0 55 mnp — Channel 5 must be inactive prior to use of this command. Upon activating sampling and conversion of the multiplexer, channel mnp is initiated, followed by sequential sampling and conversion of successive (increasing) multiplexer channels until Channel 5 becomes inactive. Transfer is under channel free-cycle control. When Channel 5 is activated again, the first multiplexer address is the mnp of the last instruction programmed (stored in the U register).

74 0 55, m+4, np — Same as 74 0 55 mnp except that, upon reactivating Channel 5 after the initial sample group, the multiplexer channel succeeding the one last sampled will be the first sampled of the next group.

74 0 56 mnp — Same as 74 0 55 mnp except that the group length is determined by (mnp+1) of 74 0 56, m+4, np or channel inactive, whichever occurs first, and starts on the first clock pulse after the buffer becomes active. If buffer remains active, a new group starting at the previous start point (mnp of this instruction) will begin on the next clock pulse proceeding at free-cycle transfer rate until the number of successive samples determined by mnp of 74 0 56, m+4, np has been made. Maximum mnp $= 159_{10}$.

74 0 56, m+4, np — Enter in the number of samples to be made for 74 0 56 mnp. For proper action, this instruction must be programmed with Channel 5 inactive. The number of samples to be made is mnp + 1. Maximum mnp $= 377_8$.

74 0 570 mn — Set clock frequency

$$F\,\frac{10^m}{n+1}\ \text{pps}\quad \text{where f = 1 to 9}$$

except when m = 6, $\frac{16}{n+1}$ pps

$$m = 7,\ \frac{\text{external source}}{n+1}\ \text{pps}$$

74 0 57100 Set clock frequency to switch setting

74 0 57200 Start clock
7201 Start clock on next second tick
7202 Stop clock

NOTE: These instructions also apply for external source.

74 0 57300 Clear DC Calibrator
7301 Set calibrator input to +10 V
7302 Set calibrator input to +5 V
7303 Set calibrator input to +2.5 V
7304 Set calibrator input to 0 V
7305 Set calibrator input to -2.5 V
7306 Set calibrator input to -5 V
7307 Set calibrator input to -10 V

74 0 57400 Select spare A

FUNCTION SELECT CODES FOR CHANNEL 6

74 0 60000 Master clear

74 0 64000 Interrupt on clock rate excessive
4001 Remove interrupt selection above
4002 Interrupt on OC2
4003 Remove interrupt selection above
4004 Interrupt on OC3
4005 Remove interrupt selection above
4006 Interrupt on OC4
4007 Remove interrupt selection above

74 0 64100 Remove all interrupt selections above

74 0 64200 Clear interrupt for clock rate excessive
4201 Clear interrupt for OC2
4202 Clear interrupt for OC3
4203 Clear interrupt for OC4

74 0 64300 Clear all interrupts

74 0 6500n Select D/A channel n+1 (for digital-to-analog conversion), for n = 0 to 5. If n = 6 or 7, the least significant octal digit of the word outputed selects the D/A channel for that word. In the latter case selection by the least significant digit m is D/A channel m+1 for m = 0 to 5.

74 0 6510n Same as 74 0 6500n except data (upper 12 bits is outputed to D/A converter, one word on every clock pulse).

74 0 6520n Same as 74 0 6510n except two successive words for a channel pair, i.e., D/A channels 1 and 2, 3 and 4, 5 and 6 on every clock pulse; odd channel first n may take on value of 0, 2, 4, 6. When n = 6 the two channels are selected by the least significant octal digit of the word outputed. Any two channels may be selected in this manner.

74 0 67400 Select spare A

NOTE: For 74 0 6520n, if n = 1, 3, 5, or 7, n will be normalized back to 0, 2, 4, 6.

SENSE CODES FOR CHANNEL 5

74 7 54000 Skip exit on interrupt for clock pulse
4001 Skip exit on no interrupt for clock pulse
4002 Skip exit on interrupt for clock rate excessive
4003 Skip exit on no interrupt for clock rate excessive
4004 Skip exit on interrupt for IC1
4005 Skip exit on no interrupt for IC1
4006 Skip exit on interrupt for IC2
4007 Skip exit on no interrupt for IC2

74 7 54200 Skip exit for variable clock running
4201 Skip exit for variable clock stopped
4202 Skip exit for T register counting
4203 Skip exit for T register not counting

4204 Skip exit for IC1 true
4205 Skip exit for IC1 false
4206 Skip exit for IC2 true
4207 Skip exit for IC2 false

SENSE CODES FOR CHANNEL 6

74 7 64000 Skip exit on interrupt for clock rate excessive
4001 Skip exit on no interrupt for clock rate excessive
4002 Skip exit on interrupt for OC2
4003 Skip exit on no interrupt for OC2
4004 Skip exit on interrupt for OC3
4005 Skip exit on no interrupt for OC3
4006 Skip exit on interrupt for OC4
4007 Skip exit on no interrupt for OC4

74 7 64200 Skip exit for clock rate excessive true
4201 Skip exit for clock rate excessive false
4202 Skip exit for OC2 true
4203 Skip exit for OC2 false
4204 Skip exit for OC3 true
4205 Skip exit for OC3 false
4206 Skip exit for OC4 true
4207 Skip exit for OC4 false

SELECT INSTRUCTION FOR CHANNEL 5

NOTE: For proper control, Channel 5 must be inactive prior to execution of these select instructions.

74 0 55 mnp

1. Select code reads mnp of this instruction into the U register. Then (U) → V.
2. Upon activating Channel 5, output address set and (U) → V.
3. Input resume increments the V register and outputs address set until Channel 5 becomes inactive. The V register recycles to 0 after a count of 159_{10}.
4. Upon reactivating Channel 5, repeat Step 2, etc.

74 0 55, m+4, np

1. Select code reads mnp of this instruction into U, then (U) → V.
2. Upon activating Channel 5, output address set.
3. Input resume increments V register and outputs address set until Channel 5 becomes inactive. The V register recycles to 0 after a count of 159_{10}.
4. Upon reactivating Channel 5, repeat Step 2, etc.

74 0 56 mnp

1. Select code reads mnp of this instruction into U register. Then (U) → V.
2. Upon activating Channel 5, no change.

3. On first clock pulse after Step 2 is completed, (U) → V, (S) → T, and output address set.

4. Input resume increments V and T registers and outputs address set until Channel 5 is inactive or T is 0, whichever occurs first. The V register recycles to 0 after 159_{10}. The T register recycles to 0 after 2^8-1.

5. If any clock pulse occurs before T = 0, an interrupt signal is sent to an interrupt flip-flop. The first clock pulse occurring after T = 0 repeats Step 3, etc.

74 0 56 m+4 np

1. Select code reads mnp of this instruction into the S register.

SELECT INSTRUCTION FOR CHANNEL 6

NOTE: For normal operation Channel 6 must be inactive prior to execution of these select functions.

74 0 6500n

1. The select code of this instruction selects the D/A channel, which is determined by the value of n (and possibly three lowest-order bits of output word; Step 4).

2. Upon activating channel, information on output buffer lines will be converted, under channel free-cycle control until the channel becomes inactive.

3. If more than one word is buffered, the same channel will be used until changed by selecting a different value for n.

4. If n = 6 or 7, the three lowest-order bits of output lines will select the channel.

74 0 6510n

1. The select code of this instruction selects the D/A channel, which is determined by the value of n as for 74 0 6500n.

2. Upon activating Channel 6, no change.

3. On the first clock pulse after the channel becomes active, information on the output lines is converted. If more than one word is selected, information will be converted one word on each clock pulse until the channel becomes inactive. (See note on next page.)

74 0 6520n

1. The value of n for this instruction selects the D/A channel pair.

2. Upon activating Channel 6, no change.

3. On the first clock pulse after Channel 6 becomes active, the first word will be converted on the odd channel. On receipt of an output resume, the second word will be converted on the even channel. At the next clock pulse, the same procedure repeats, starting again with the odd channel as above until the channel becomes inactive. (See note on next page.)

4. If n = 6 or 7, the three lowest-order bits of the output buffer lines will select the channel when in the above instruction n = 6 or 7; the lowest-order bits may select the channels in any order.

NOTE: For 74 0 6510n and 74 0 6520n, if the processes defined in Step 3 are not completed before the next clock pulse, an interrupt signal is sent to an interrupt flip-flop. Repetition of the processes is initiated on the first clock pulse following completion of previous action.

Appendix C

COMPUTER-INTERFACE I/O BUFFER TIMING

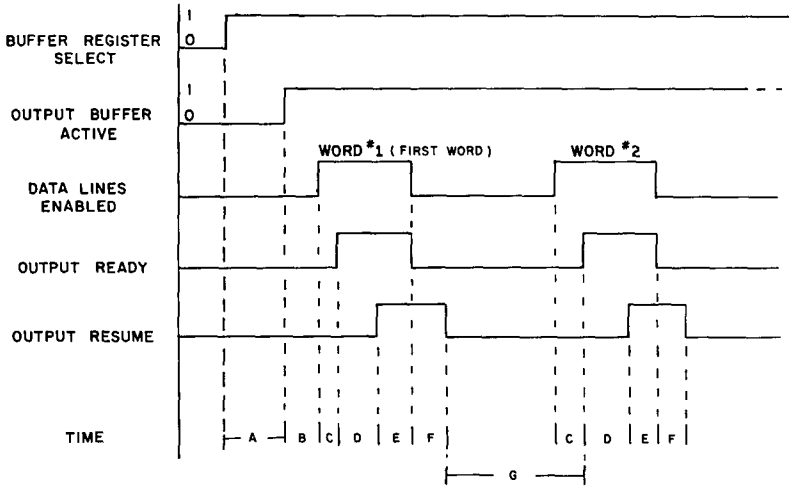

Fig. C1 - Computer-interface output timing

PERIOD A - Period before computer program activates output channel after selecting the buffer register.

B - 6.0 μsec - 9.4 μsec (one channel active).
6.0 μsec - 44.0 μsec (all channels active).

C - 1.2 μsec.

D - Determined by external equipment.

E - Time from when external equipment sends output resume until computer drops the output ready and clears output lines 2.0 μsec to 4.0 μsec.

F - Determined by external equipment.

G - One output channel active 6.0 μsec to 12.0 μsec, all channels active and demand processing 6.0 μsec to 44.0 μsec (remainder of channels are in 924 mode).

74 0 45700 Stop and reset reverse clock and select preset
5701 Start reverse clock
5702 Stop reverse clock

74 0 4600n Select cyclic D/A block starting at D/A channel n+1; $0 \leq n \leq 5$ (antenna error, D/A channels 1 and 2 for az and el)

74 0 46100 Take one frame on Flight Research camera

SENSE CODES FOR CHANNEL 3

74 7 34000 Skip exit on interrupt for sample time
4001 Skip exit on no interrupt for sample time
4002 Skip exit on interrupt for subsample time
4003 Skip exit on no interrupt for subsample time
4004 Skip exit on interrupt for subsample time
4005 Skip exit on no interrupt for subsample time
4006 Skip exit on interrupt for elevation angle ready
4007 Skip exit on no interrupt for elevation angle ready
4010 Skip exit on interrupt for both azimuth and elevation ready
4011 Skip exit on no interrupt for both azimuth and elevation ready
4012 Skip exit on interrupt for D/R ready to input
4013 Skip exit on no interrupt for D/R ready to input
4014 Skip exit on forced interrupt
4015 Skip exit on no forced interrupt
4016 Skip exit on interrupt for strobe pulse
4017 Skip exit on no interrupt for strobe pulse

74 7 35000 Skip exit on sample time true
5001 Skip exit on sample time false
5002 Skip exit on subsample time true
5003 Skip exit on subsample time false
5004 Skip exit on azimuth angle held in register
5005 Skip exit on azimuth angle being digitized
5006 Skip exit on elevation angle held in register
5007 Skip exit on elevation angle being digitized
5010 Skip exit on azimuth and elevation angles held in registers
5011 Skip exit on azimuth and elevation angles being digitized
5012 Skip exit on D/R inactive
5013 Skip exit on D/R active
5014 Skip exit on slave input ready (IC1)
5015 Skip exit on slave input not ready (IC1)
5016 Skip exit on condition strobe pulse true
5017 Skip exit on condition no strobe pulse

SENSE CODES FOR CHANNEL 4

74 7 44000 Skip exit on interrupt for receiver No. 1 above track threshold
4001 Skip exit on no interrupt for receiver No. 1 above track threshold
4002 Skip exit on interrupt for receiver No. 2 above track threshold
4003 Skip exit on no interrupt for receiver No. 2 above track threshold
4004 Skip exit on interrupt for reverse clock all zeros
4005 Skip exit on no interrupt for reverse clock all zeros
4006 Skip exit on interrupt for slave out request (OC1)

4007 Skip exit on no interrupt for slave out request (OC1)
4010 Skip exit on interrupt for OC2
4011 Skip exit on no interrupt for OC2
4012 Skip exit on interrupt for OC3
4013 Skip exit on no interrupt for OC3
4014 Skip exit on interrupt for OC4
4015 Skip exit on no interrupt for OC4
4016 Skip exit on interrupt for OC5
4017 Skip exit on no interrupt for OC5

74 7 45000 Skip exit for receiver No. 1 above track threshold
5001 Skip exit for receiver No. 1 below track threshold
5002 Skip exit for receiver No. 2 above track threshold
5003 Skip exit for receiver No. 2 below track threshold
5004 Skip exit for reverse clock all zeros
5005 Skip exit for reverse clock not all zeros
5006 Skip exit for slave out request (OC1) true
5007 Skip exit for slave out request (OC1) false
5010 Skip exit for OC2 true
5011 Skip exit for OC2 false
5012 Skip exit for OC3 true
5013 Skip exit for OC3 false
5014 Skip exit for OC4 true
5015 Skip exit for OC4 false
5016 Skip exit for OC5 true
5017 Skip exit for OC5 false

74 7 45300 Skip exit for camera single-frame mode
5301 Skip exit for camera not single-frame mode

74 7 45400 Skip exit for camera open-shutter mode
5401 Skip exit for camera not open-shutter mode

74 7 46000 Skip exit for camera shutter open
6001 Skip exit for camera shutter closed

FUNCTION SELECT CODES FOR CHANNEL 5

74 0 50000 Master clear - clears all Channel 5 equipment and interrupt selections, clears all interrupt signals, and sets appropriate clear and zero indications.

74 0 54000 Interrupt on clock pulse
4001 Remove interrupt selection above
4002 Interrupt on clock rate excessive for 74056 mnp
4003 Remove interrupt selection above
4004 Interrupt on input condition 1 (IC1)
4005 Remove interrupt selection above
4006 Interrupt on input condition 2 (IC2)
4007 Remove interrupt selection above

74 0 54100 Remove all interrupt selections

74 0 54200 Clear interrupt for clock pulse
4201 Clear interrupt for clock rate excessive
4202 Clear interrupt for IC1
4203 Clear interrupt for IC2

74 0 54300 Clear all interrupts

74 0 55 mnp Channel 5 must be inactive prior to use of this command. Upon activating sampling and conversion of the multiplexer, channel mnp is initiated, followed by sequential sampling and conversion of successive (increasing) multiplexer channels until Channel 5 becomes inactive. Transfer is under channel free-cycle control. When Channel 5 is activated again, the first multiplexer address is the mnp of the last instruction programmed (stored in the U register).

74 0 55, m+4, np Same as 74 0 55 mnp except that, upon reactivating Channel 5 after the initial sample group, the multiplexer channel succeeding the one last sampled will be the first sampled of the next group.

74 0 56 mnp Same as 74 0 55 mnp except that the group length is determined by (mnp+1) of 74 0 56, m+4, np or channel inactive, whichever occurs first, and starts on the first clock pulse after the buffer becomes active. If buffer remains active, a new group starting at the previous start point (mnp of this instruction) will begin on the next clock pulse proceeding at free-cycle transfer rate until the number of successive samples determined by mnp of 74 0 56, m+4, np has been made. Maximum mnp = 159_{10}.

74 0 56, m+4, np Enter in the number of samples to be made for 74 0 56 mnp. For proper action, this instruction must be programmed with Channel 5 inactive. The number of samples to be made is mnp + 1. Maximum mnp = 377_8.

74 0 570 mn Set clock frequency

$$F\,\frac{10^m}{n+1}\ \text{pps}\quad \text{where f = 1 to 9}$$

except when m = 6, $\frac{16}{n+1}$ pps

m = 7, $\frac{\text{external source}}{n+1}$ pps

74 0 57100 Set clock frequency to switch setting

74 0 57200 Start clock
7201 Start clock on next second tick
7202 Stop clock

NOTE: These instructions also apply for external source.

74 0 57300 Clear DC Calibrator
7301 Set calibrator input to +10 V
7302 Set calibrator input to +5 V
7303 Set calibrator input to +2.5 V
7304 Set calibrator input to 0 V
7305 Set calibrator input to -2.5 V
7306 Set calibrator input to -5 V
7307 Set calibrator input to -10 V

74 0 57400 Select spare A

FUNCTION SELECT CODES FOR CHANNEL 6

74 0 60000 Master clear

74 0 64000 Interrupt on clock rate excessive
4001 Remove interrupt selection above
4002 Interrupt on OC2
4003 Remove interrupt selection above
4004 Interrupt on OC3
4005 Remove interrupt selection above
4006 Interrupt on OC4
4007 Remove interrupt selection above

74 0 64100 Remove all interrupt selections above

74 0 64200 Clear interrupt for clock rate excessive
4201 Clear interrupt for OC2
4202 Clear interrupt for OC3
4203 Clear interrupt for OC4

74 0 64300 Clear all interrupts

74 0 6500n Select D/A channel n+1 (for digital-to-analog conversion), for n = 0 to 5. If n = 6 or 7, the least significant octal digit of the word outputed selects the D/A channel for that word. In the latter case selection by the least significant digit m is D/A channel m+1 for m = 0 to 5.

74 0 6510n Same as 74 0 6500n except data (upper 12 bits is outputed to D/A converter, one word on every clock pulse).

74 0 6520n Same as 74 0 6510n except two successive words for a channel pair, i.e., D/A channels 1 and 2, 3 and 4, 5 and 6 on every clock pulse; odd channel first n may take on value of 0, 2, 4, 6. When n = 6 the two channels are selected by the least significant octal digit of the word outputed. Any two channels may be selected in this manner.

74 0 67400 Select spare A

NOTE: For 74 0 6520n, if n = 1, 3, 5, or 7, n will be normalized back to 0, 2, 4, 6.

SENSE CODES FOR CHANNEL 5

74 7 54000 Skip exit on interrupt for clock pulse
4001 Skip exit on no interrupt for clock pulse
4002 Skip exit on interrupt for clock rate excessive
4003 Skip exit on no interrupt for clock rate excessive
4004 Skip exit on interrupt for IC1
4005 Skip exit on no interrupt for IC1
4006 Skip exit on interrupt for IC2
4007 Skip exit on no interrupt for IC2

74 7 54200 Skip exit for variable clock running
4201 Skip exit for variable clock stopped
4202 Skip exit for T register counting
4203 Skip exit for T register not counting

4204 Skip exit for IC1 true
4205 Skip exit for IC1 false
4206 Skip exit for IC2 true
4207 Skip exit for IC2 false

SENSE CODES FOR CHANNEL 6

74 7 64000 Skip exit on interrupt for clock rate excessive
4001 Skip exit on no interrupt for clock rate excessive
4002 Skip exit on interrupt for OC2
4003 Skip exit on no interrupt for OC2
4004 Skip exit on interrupt for OC3
4005 Skip exit on no interrupt for OC3
4006 Skip exit on interrupt for OC4
4007 Skip exit on no interrupt for OC4

74 7 64200 Skip exit for clock rate excessive true
4201 Skip exit for clock rate excessive false
4202 Skip exit for OC2 true
4203 Skip exit for OC2 false
4204 Skip exit for OC3 true
4205 Skip exit for OC3 false
4206 Skip exit for OC4 true
4207 Skip exit for OC4 false

SELECT INSTRUCTION FOR CHANNEL 5

NOTE: For proper control, Channel 5 must be inactive prior to execution of these select instructions.

74 0 55 mnp

1. Select code reads mnp of this instruction into the U register. Then (U) → V.
2. Upon activating Channel 5, output address set and (U) → V.
3. Input resume increments the V register and outputs address set until Channel 5 becomes inactive. The V register recycles to 0 after a count of 159_{10}.
4. Upon reactivating Channel 5, repeat Step 2, etc.

74 0 55, m+4, np

1. Select code reads mnp of this instruction into U, then (U) → V.
2. Upon activating Channel 5, output address set.
3. Input resume increments V register and outputs address set until Channel 5 becomes inactive. The V register recycles to 0 after a count of 159_{10}.
4. Upon reactivating Channel 5, repeat Step 2, etc.

74 0 56 mnp

1. Select code reads mnp of this instruction into U register. Then (U) → V.
2. Upon activating Channel 5, no change.

3. On first clock pulse after Step 2 is completed, (U) → V, (S) → T, and output address set.

4. Input resume increments V and T registers and outputs address set until Channel 5 is inactive or T is 0, whichever occurs first. The V register recycles to 0 after 159_{10}. The T register recycles to 0 after 2^8-1.

5. If any clock pulse occurs before T = 0, an interrupt signal is sent to an interrupt flip-flop. The first clock pulse occurring after T = 0 repeats Step 3, etc.

74 0 56 m+4 np

1. Select code reads mnp of this instruction into the S register.

SELECT INSTRUCTION FOR CHANNEL 6

NOTE: For normal operation Channel 6 must be inactive prior to execution of these select functions.

74 0 6500n

1. The select code of this instruction selects the D/A channel, which is determined by the value of n (and possibly three lowest-order bits of output word; Step 4).

2. Upon activating channel, information on output buffer lines will be converted, under channel free-cycle control until the channel becomes inactive.

3. If more than one word is buffered, the same channel will be used until changed by selecting a different value for n.

4. If n = 6 or 7, the three lowest-order bits of output lines will select the channel.

74 0 6510n

1. The select code of this instruction selects the D/A channel, which is determined by the value of n as for 74 0 6500n.

2. Upon activating Channel 6, no change.

3. On the first clock pulse after the channel becomes active, information on the output lines is converted. If more than one word is selected, information will be converted one word on each clock pulse until the channel becomes inactive. (See note on next page.)

74 0 6520n

1. The value of n for this instruction selects the D/A channel pair.

2. Upon activating Channel 6, no change.

3. On the first clock pulse after Channel 6 becomes active, the first word will be converted on the odd channel. On receipt of an output resume, the second word will be converted on the even channel. At the next clock pulse, the same procedure repeats, starting again with the odd channel as above until the channel becomes inactive. (See note on next page.)

4. If n = 6 or 7, the three lowest-order bits of the output buffer lines will select the channel when in the above instruction n = 6 or 7; the lowest-order bits may select the channels in any order.

NOTE: For 74 0 6510n and 74 0 6520n, if the processes defined in Step 3 are not completed before the next clock pulse, an interrupt signal is sent to an interrupt flip-flop. Repetition of the processes is initiated on the first clock pulse following completion of previous action.

Appendix C

COMPUTER-INTERFACE I/O BUFFER TIMING

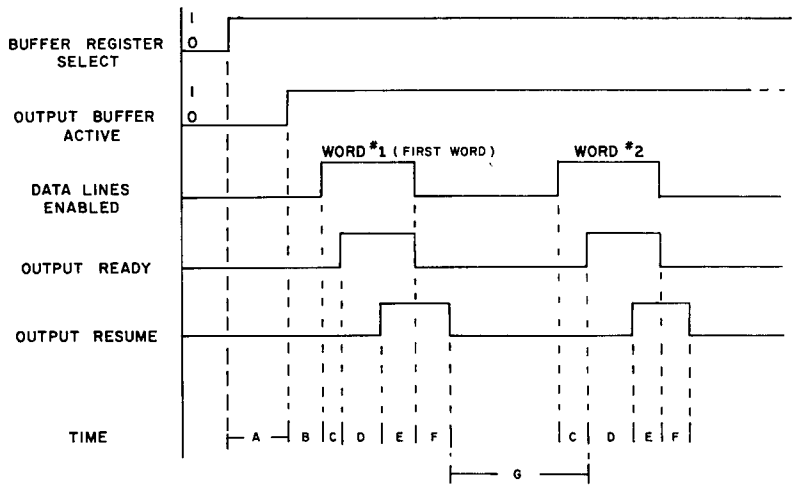

Fig. C1 - Computer-interface output timing

PERIOD A - Period before computer program activates output channel after selecting the buffer register.

B - 6.0 μsec - 9.4 μsec (one channel active).
6.0 μsec - 44.0 μsec (all channels active).

C - 1.2 μsec.

D - Determined by external equipment.

E - Time from when external equipment sends output resume until computer drops the output ready and clears output lines 2.0 μsec to 4.0 μsec.

F - Determined by external equipment.

G - One output channel active 6.0 μsec to 12.0 μsec, all channels active and demand processing 6.0 μsec to 44.0 μsec (remainder of channels are in 924 mode).

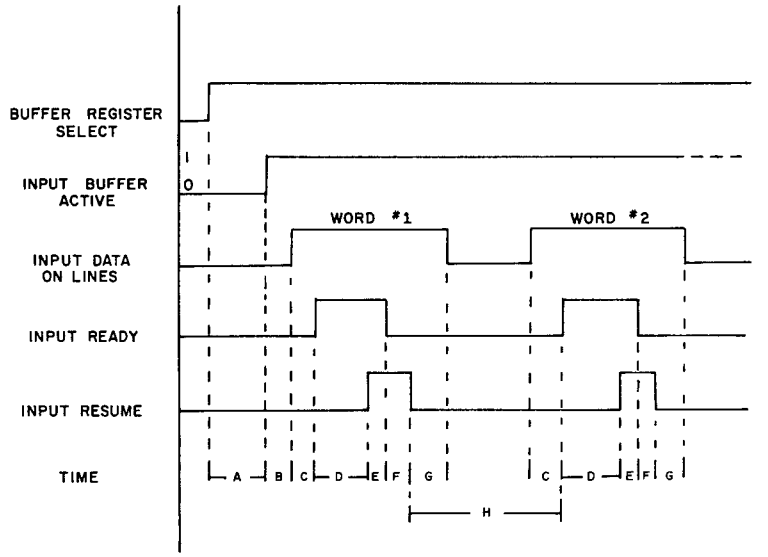

Fig. C2 - Computer-interface input timing

PERIOD A - Period before input channel is active after selecting the buffer register.
B - Determined by external equipment.
C - Determined by external equipment (input data and input ready may be sent at the same time).
D - One channel active - 6.0 μsec to 12.0 μsec (924 mode); 9.2 μsec to 12.5 μsec (1604 mode); 6.0 μsec to 44.0 μsec (all channels demand processing and all channels in 924 mode); 9.2 μsec to 63.2 μsec (all channels demand processing and all channels in 1604 mode).
E - Determined by external equipment.
F - 2.0 μsec to 4.0 μsec. This is the time from when external equipment drops the input ready signal until computer drops the input resume.
G - Determined by external equipment.
H - Determined by external equipment.

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